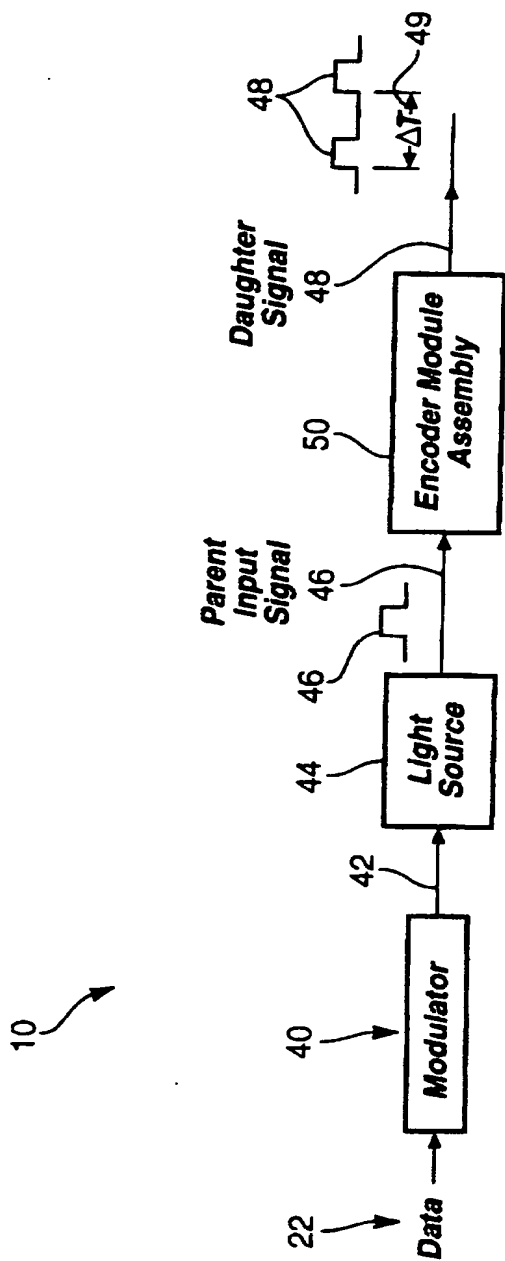


2807.2.4.10

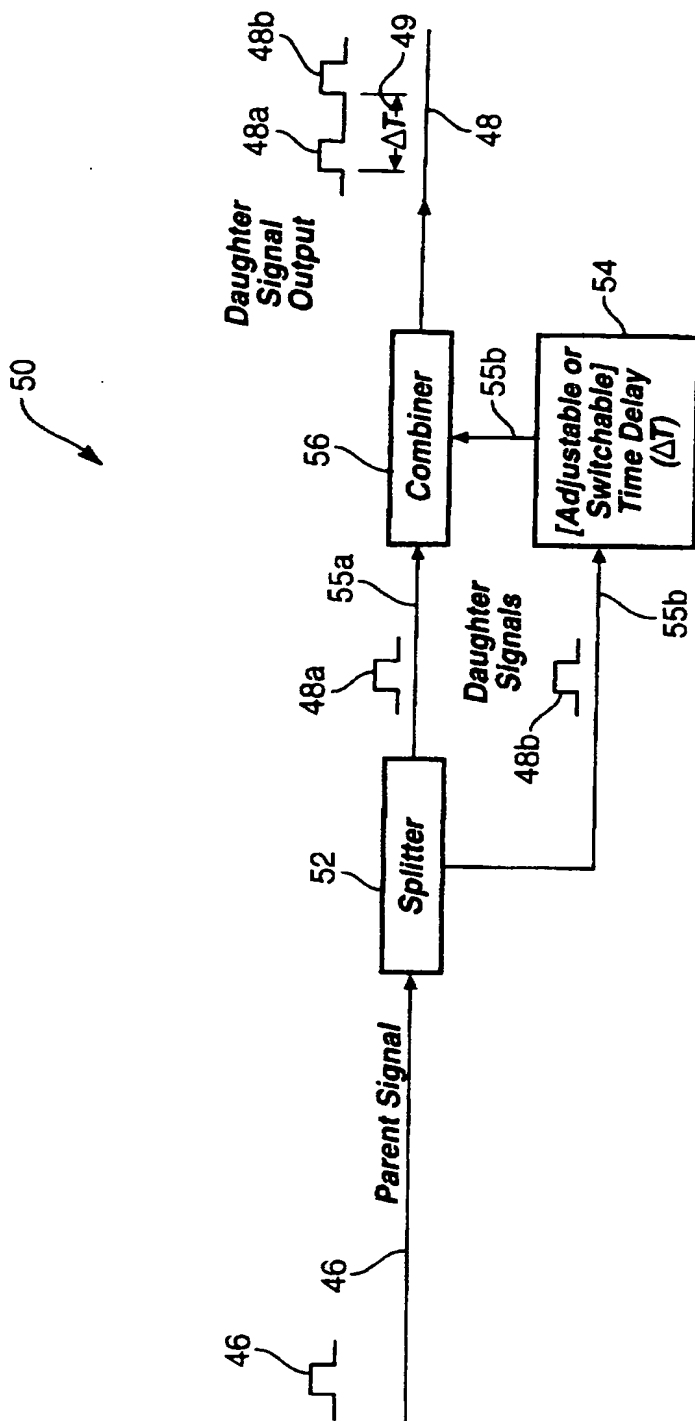




Differential Delay Multiplexer Sender/Encoder

Fig. 3

2807.2.4.10



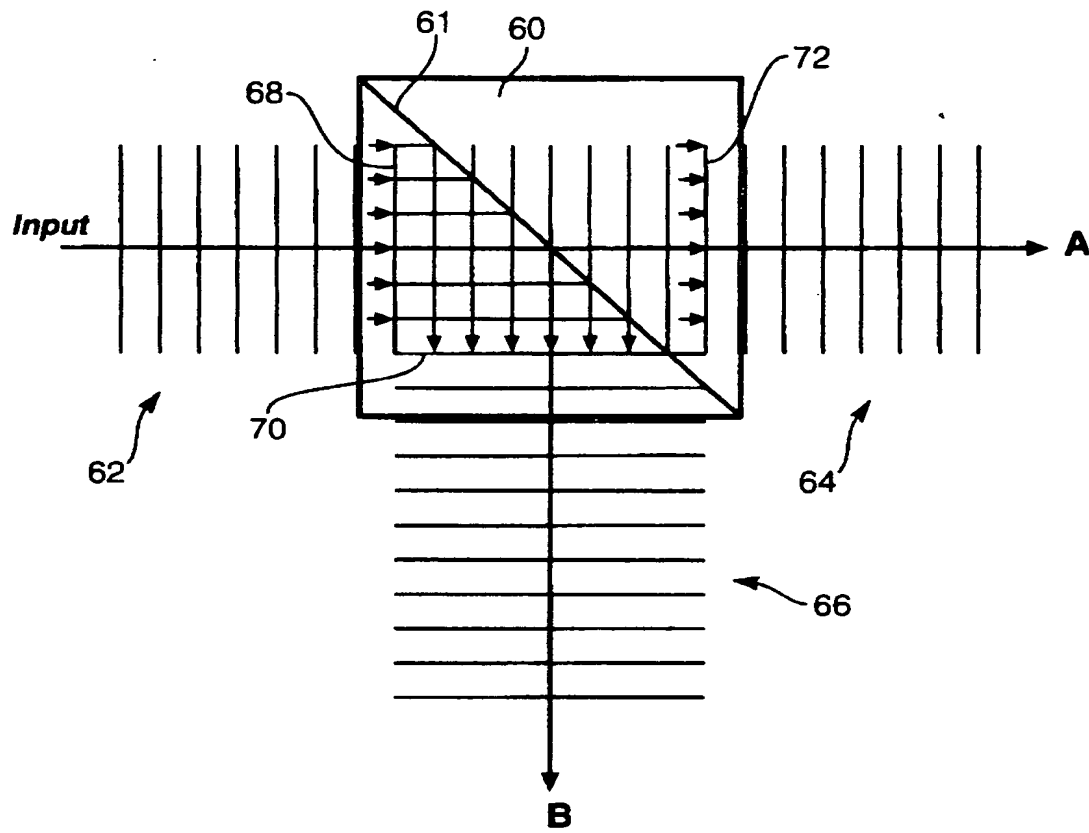
Differential Delay Multiplexer (DDM) Sender/Encoder

Fig. 4

2807.2.4.



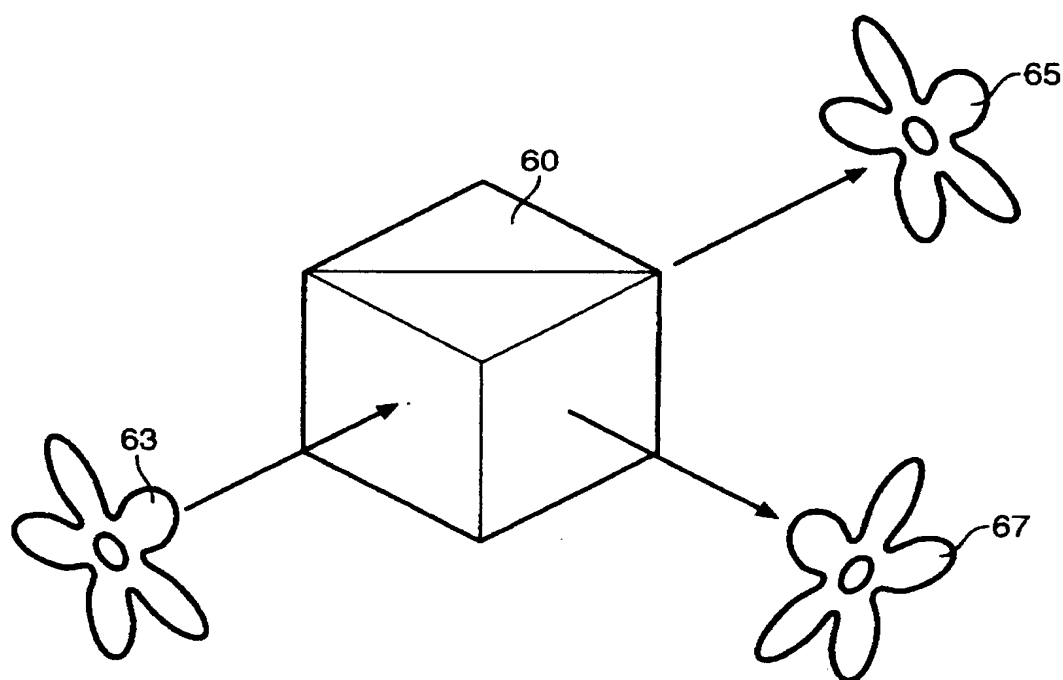
2807.2.4.



Amplitude or Polarization Splitter

FIG. 7

2807.2.4.

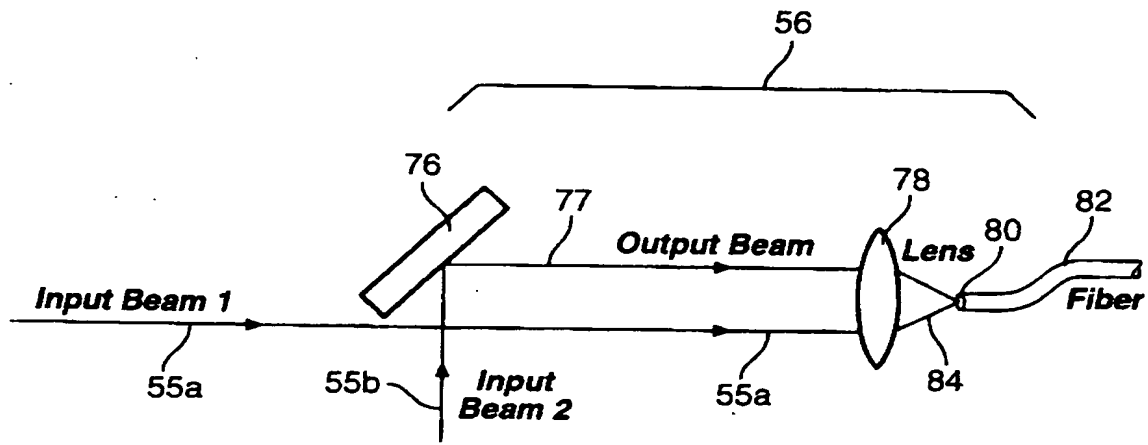


**Image Signals Which
Maintain Spatial Information**

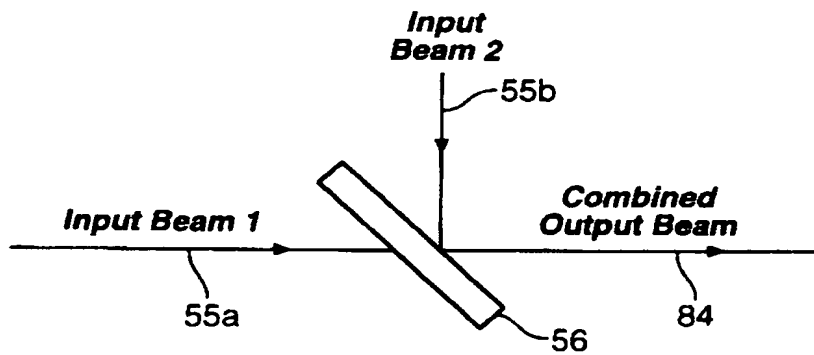
FIG. 7A

2807.2.4.

DocId:30929260



Beam Combiner
FIG. 8



Amplitude or Polarization Combiner

FIG. 9

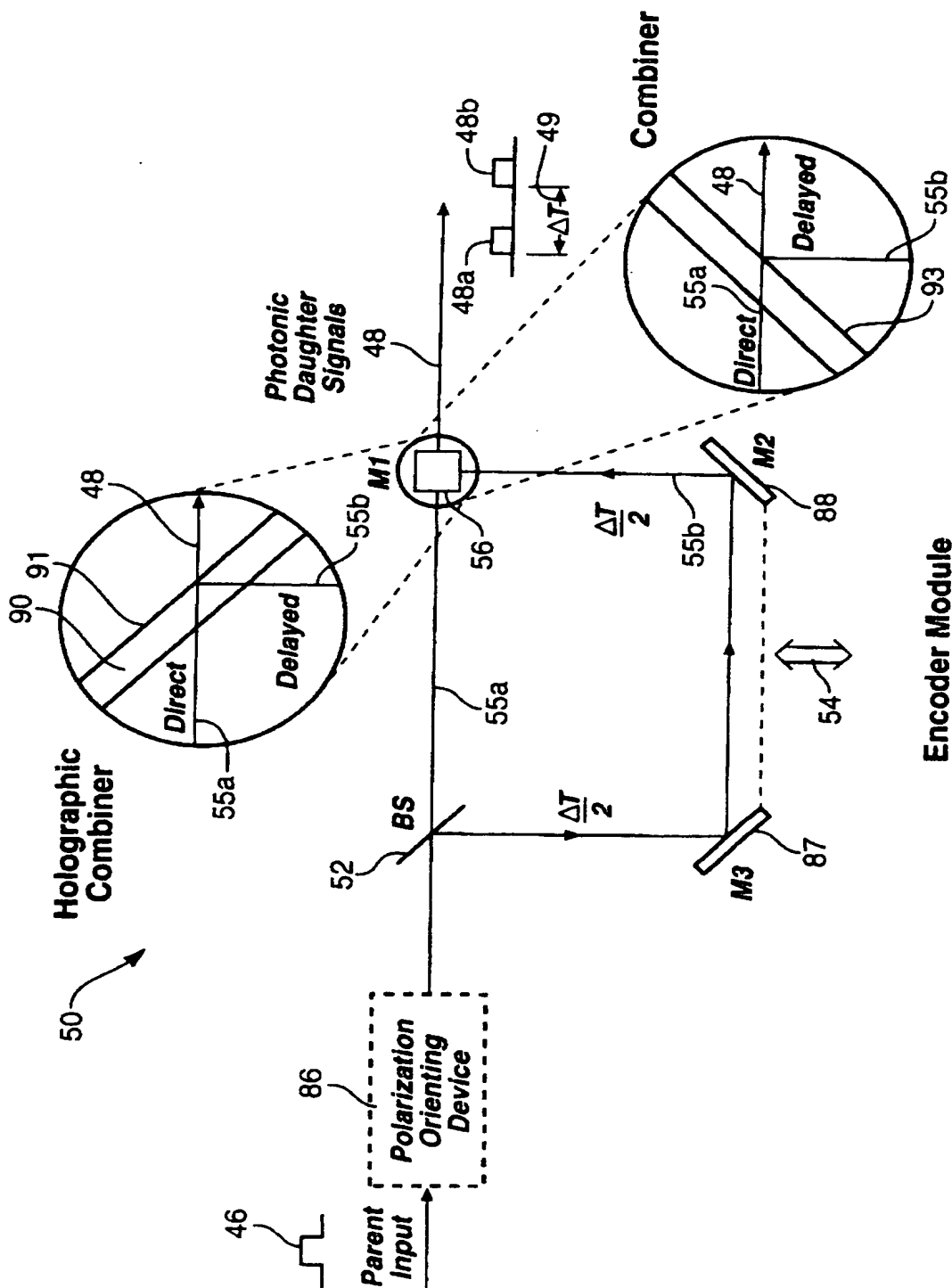
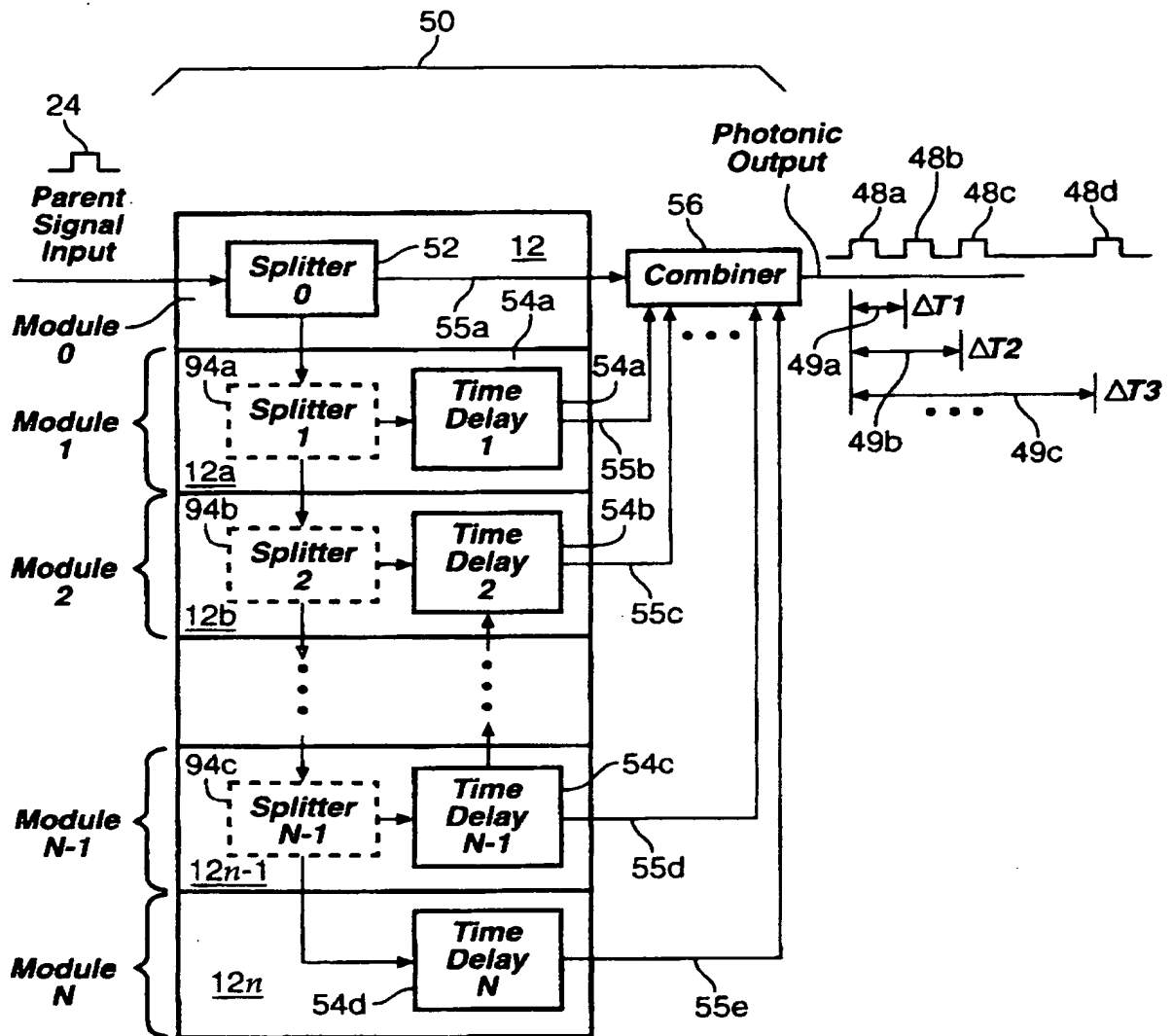


Fig. 10

2807.2.4.



Composite Encoder
Module Assembly

FIG. 11

2807.2.4.



Fig. 12

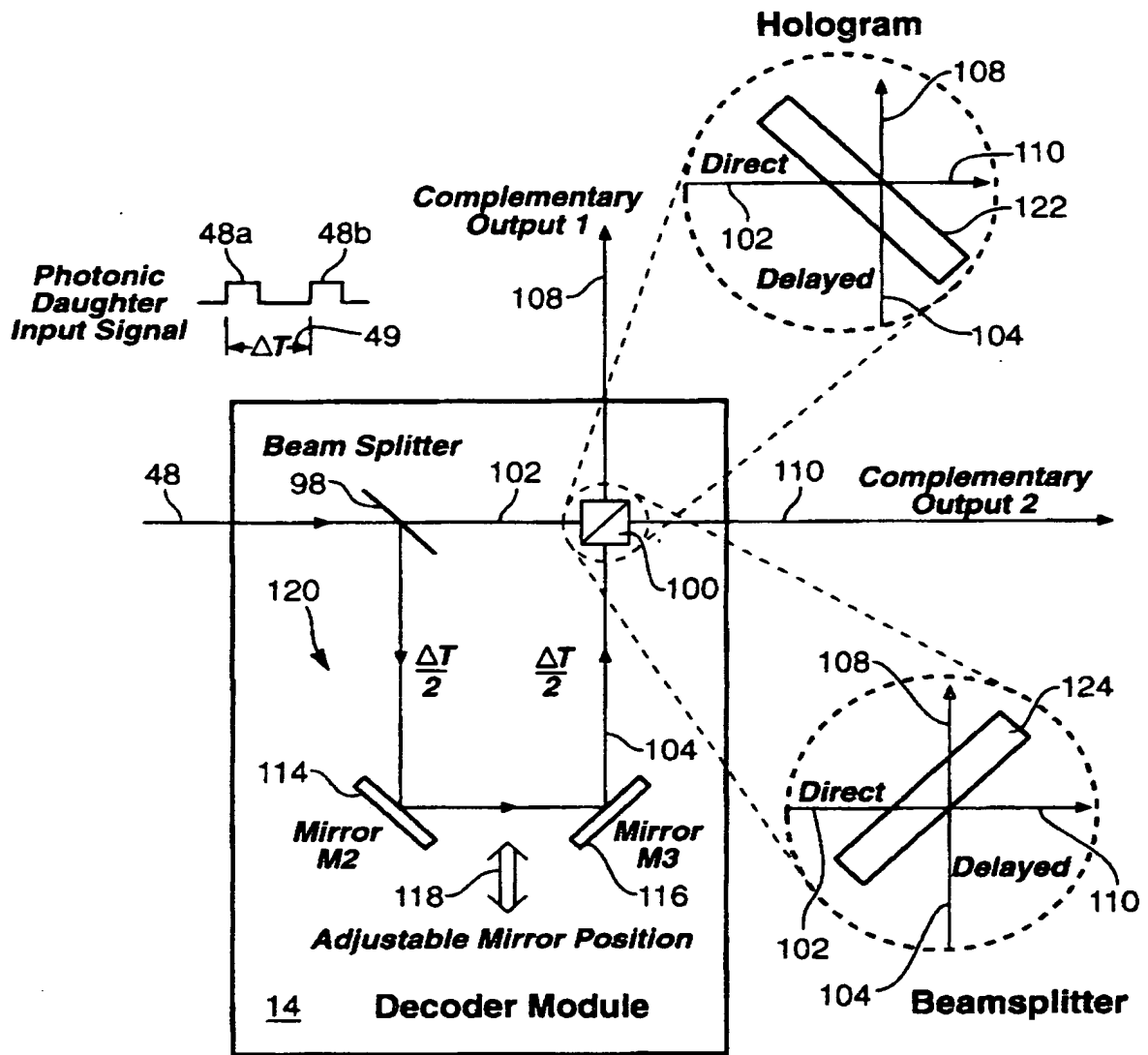


FIG. 13

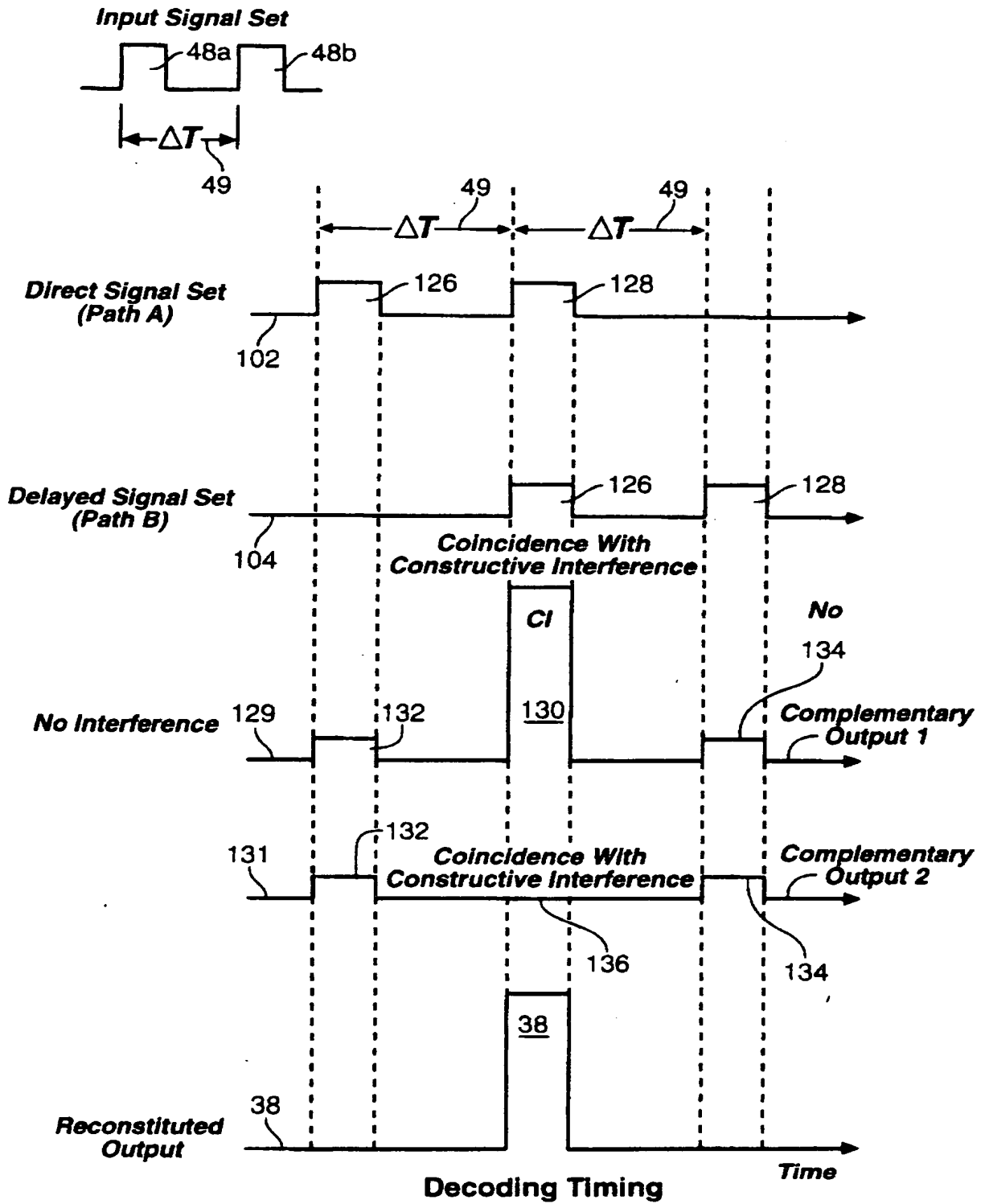


FIG. 14

48

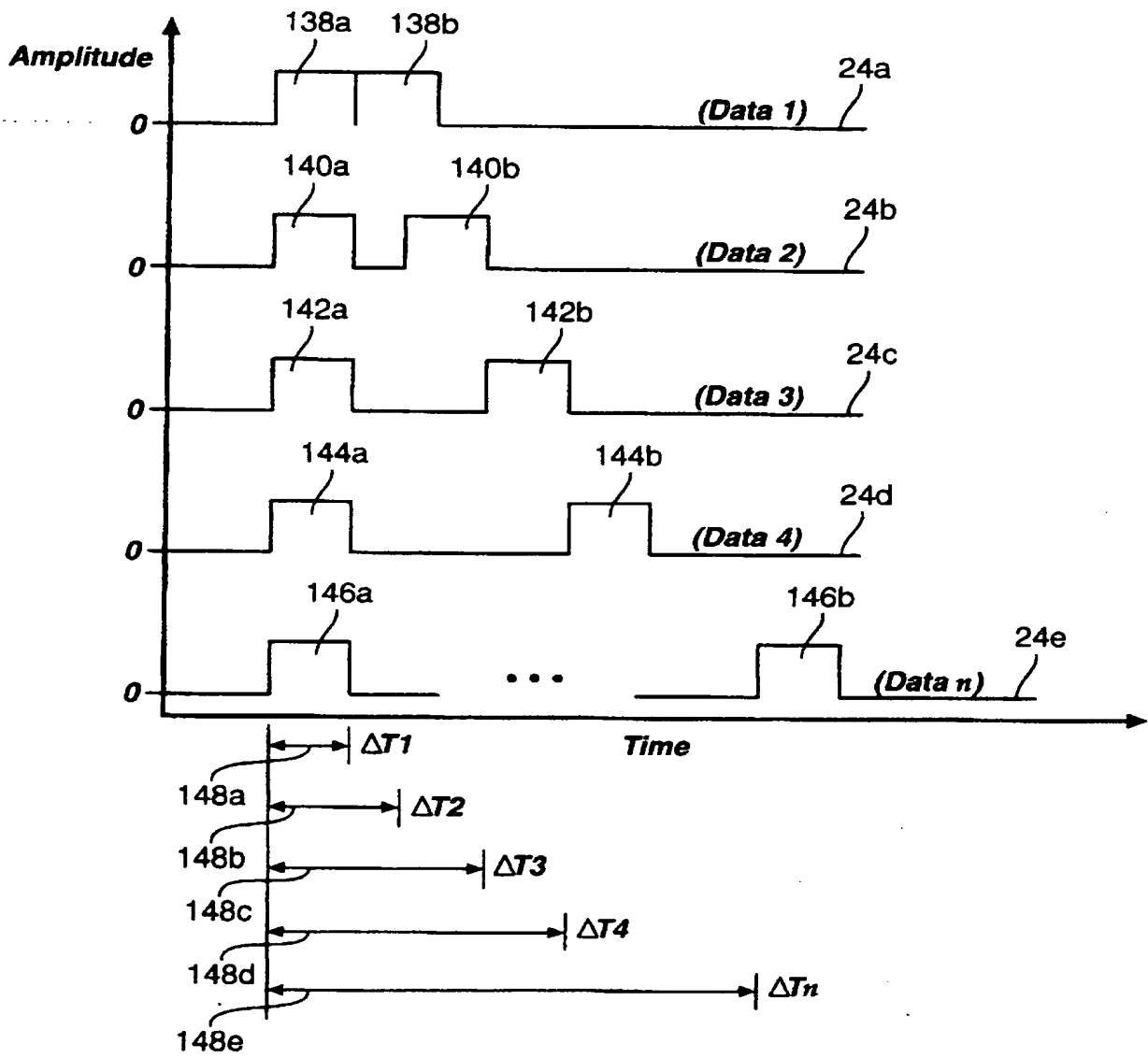


Fig. 15

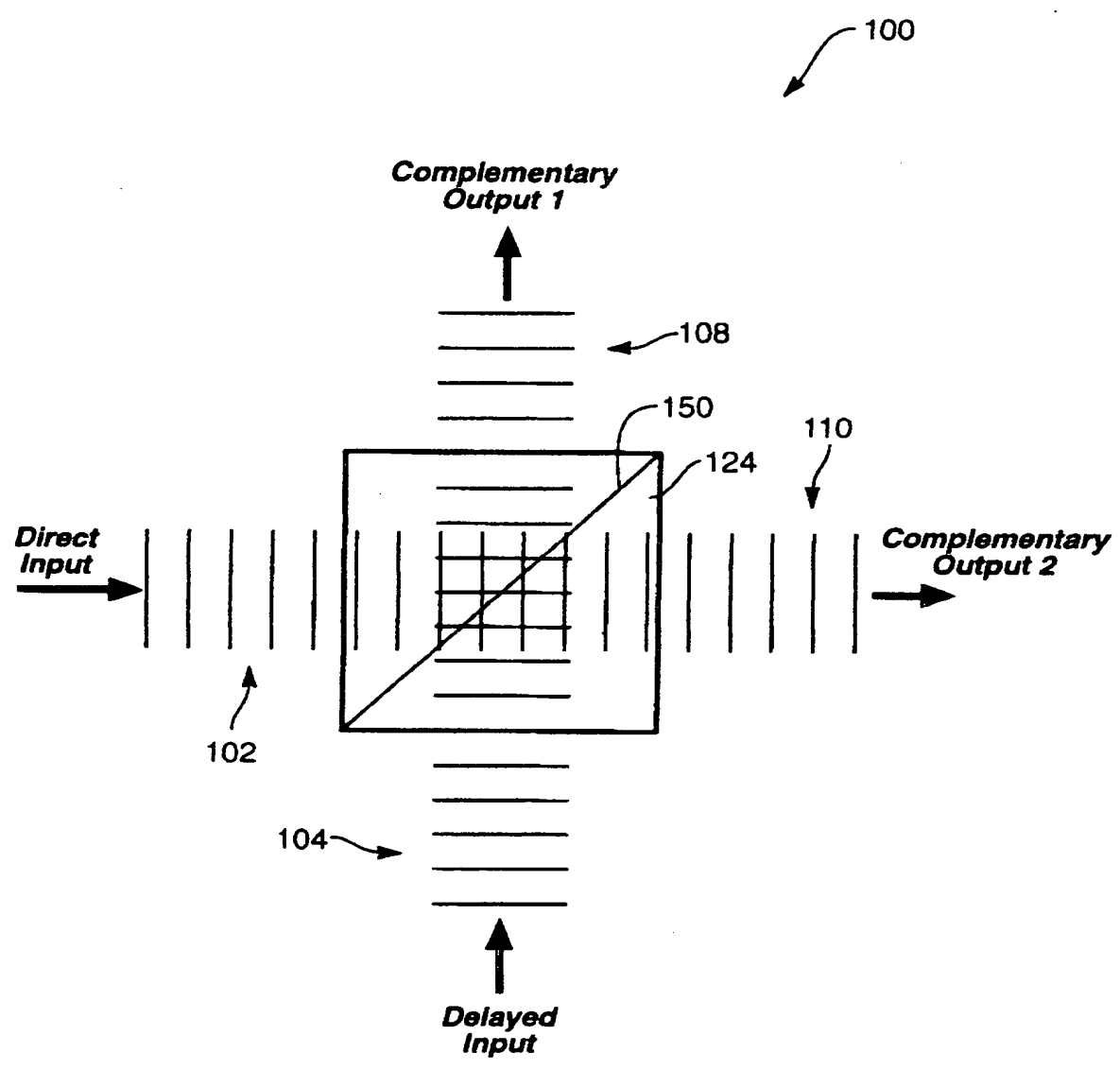


Fig. 16

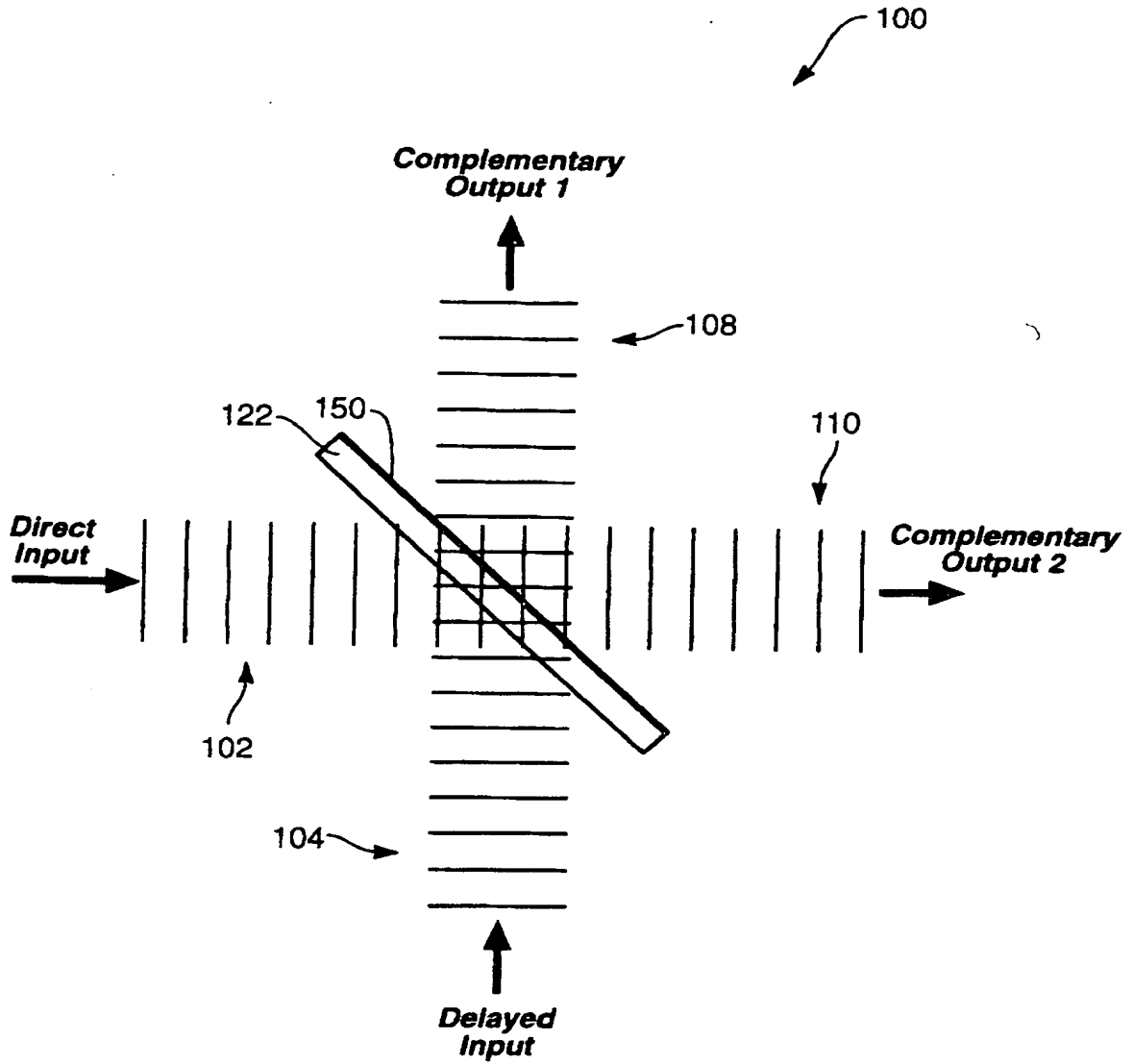


Fig. 17

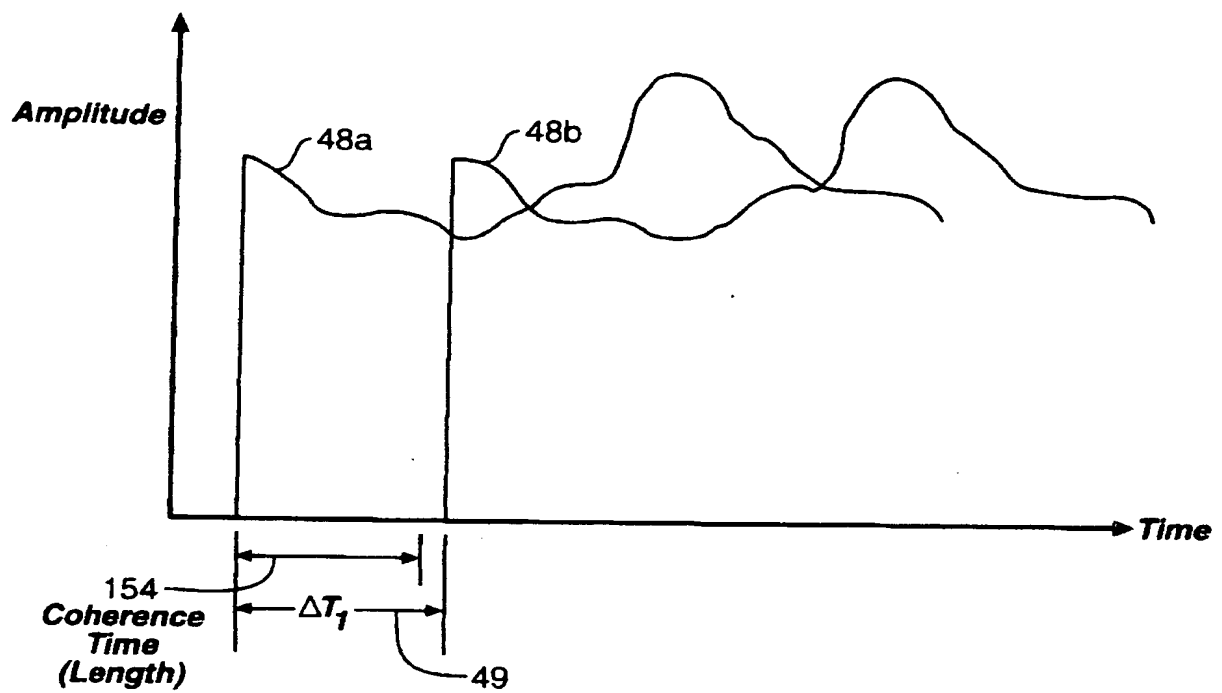


Fig. 18

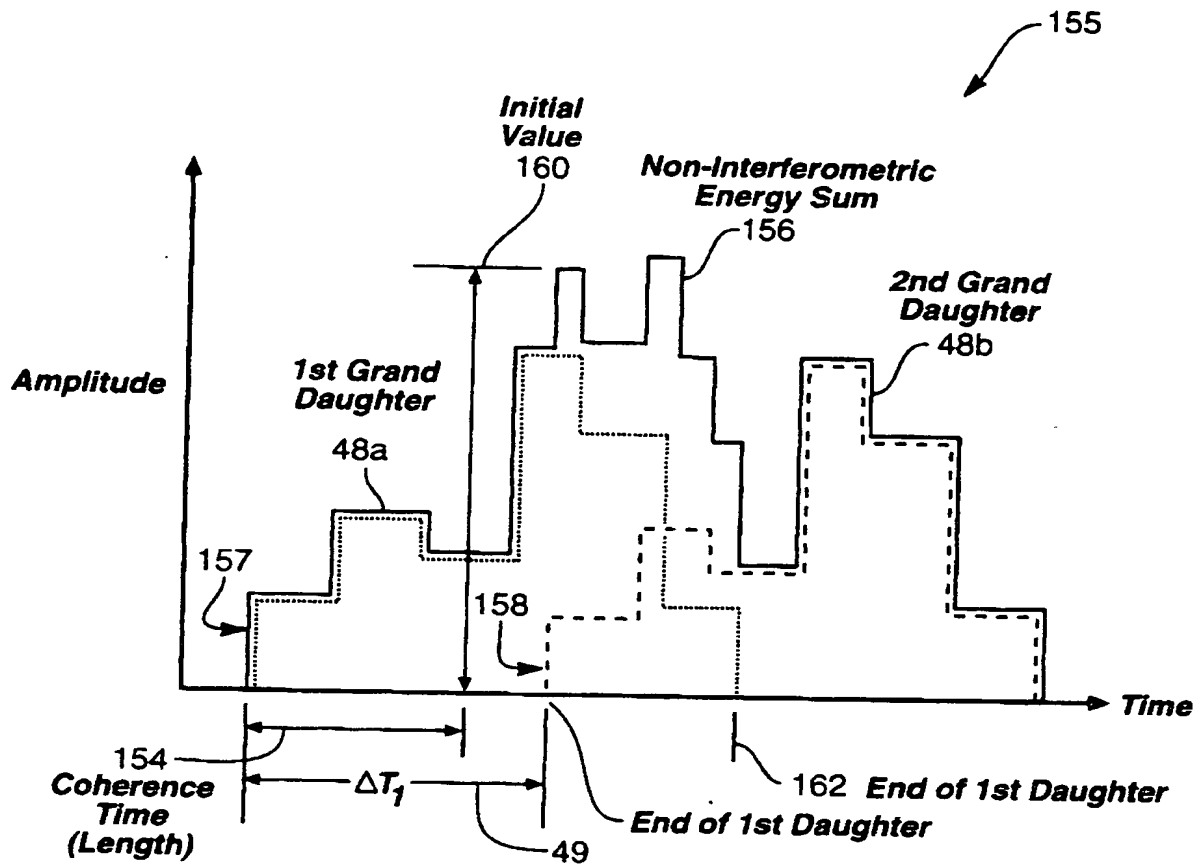


Fig. 19

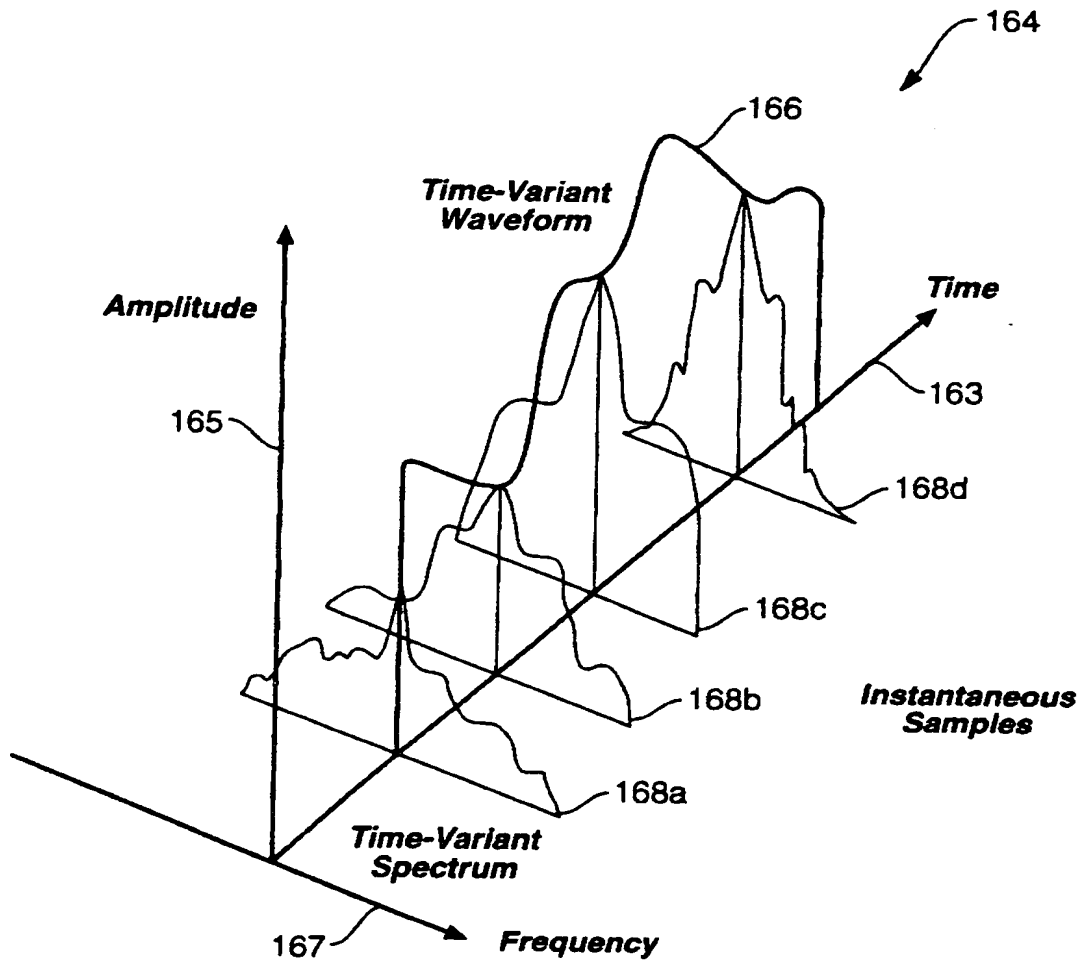
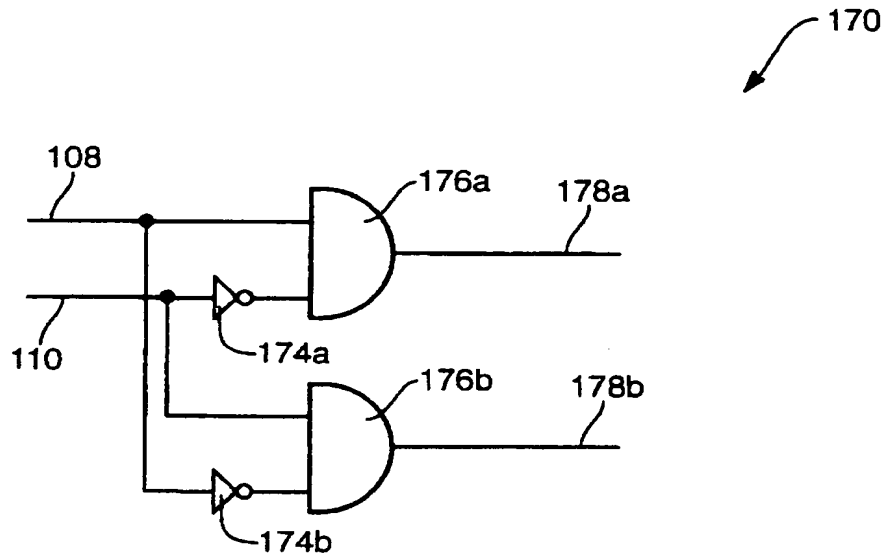
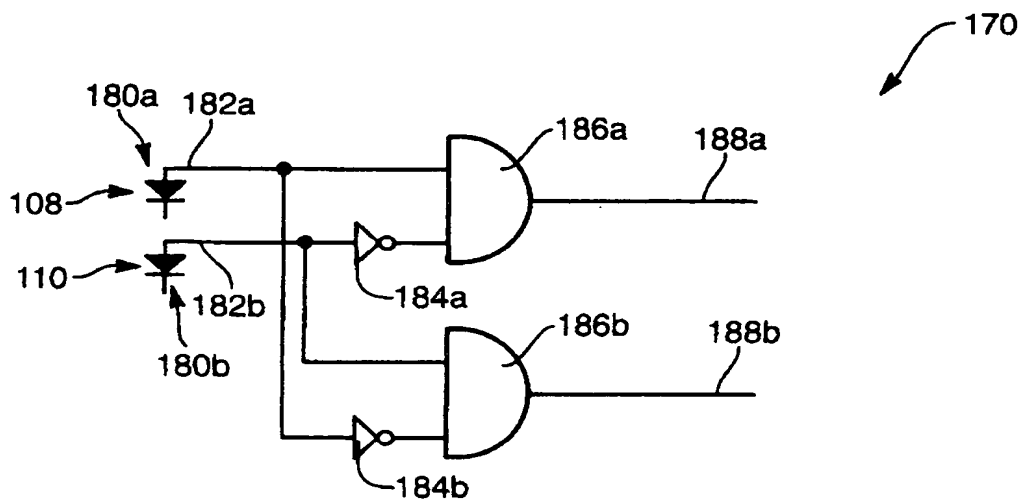


Fig. 20



Photonic Processor
Fig. 22



Electronic Processor
Fig. 23A

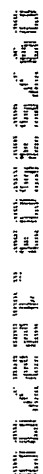
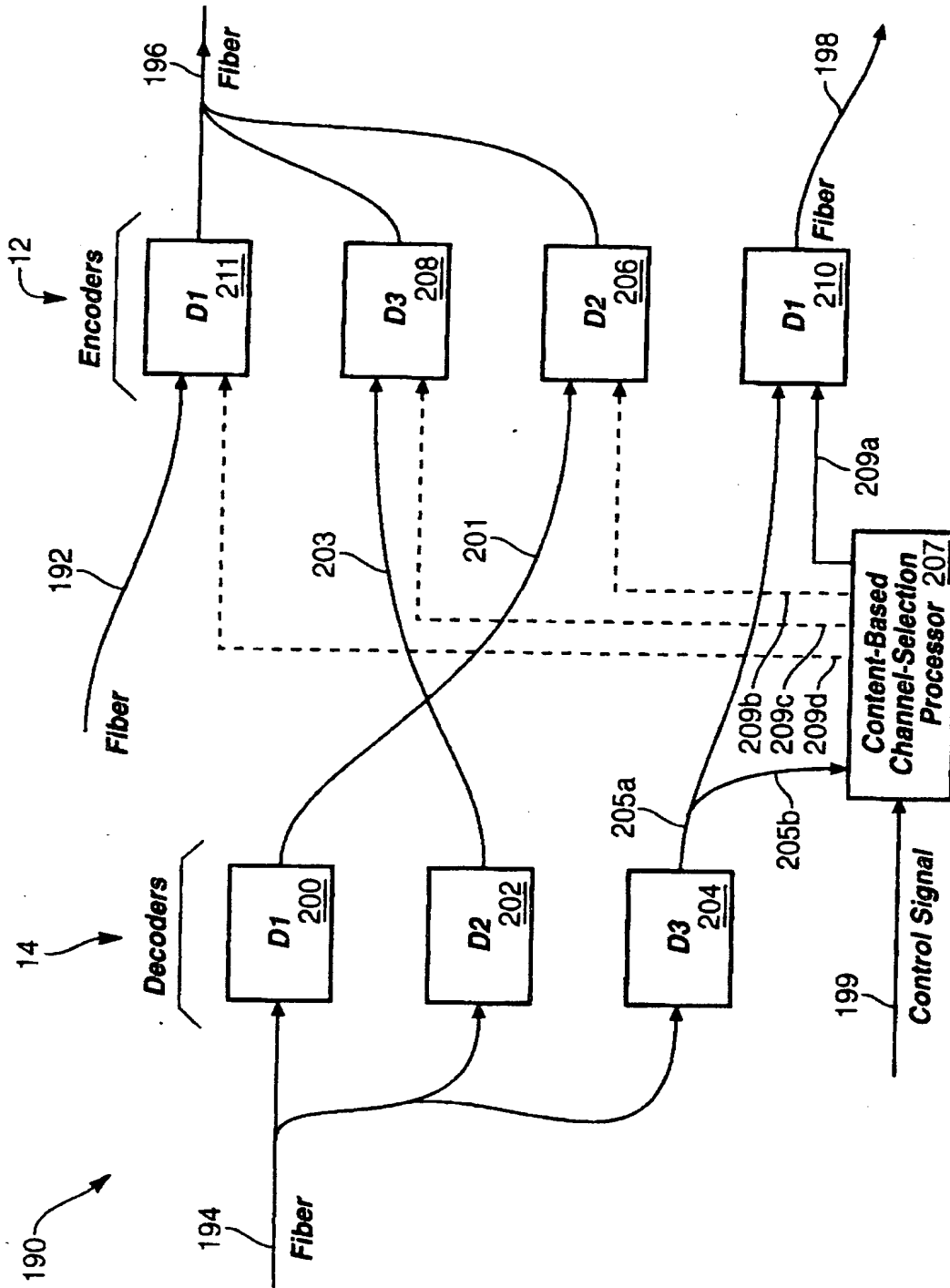
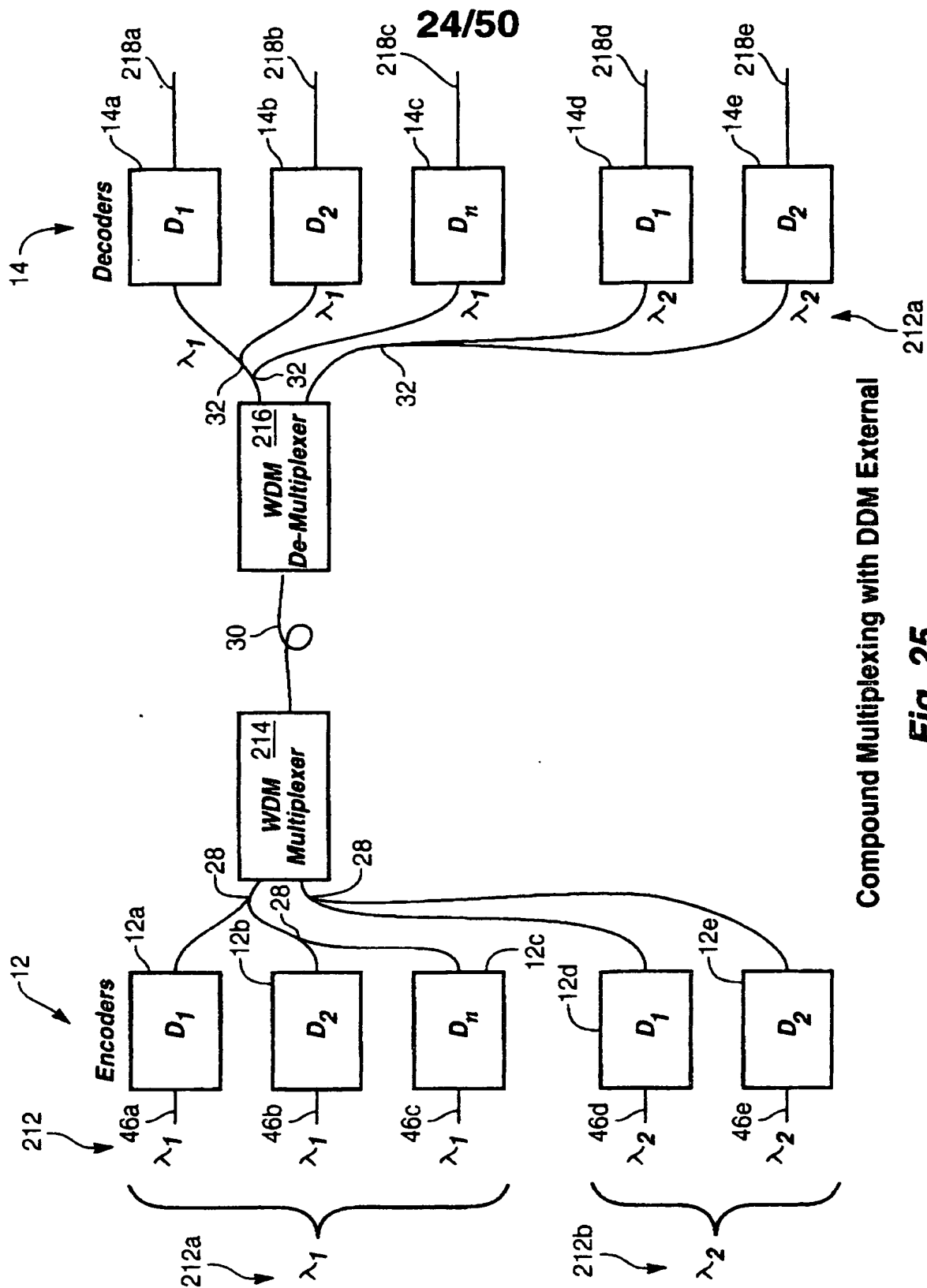


Fig. 23B



Drop/Rearrange/Add Unbuilding/Rebuilding

Fig. 24



Compound Multiplexing with DDM External

Fig. 25

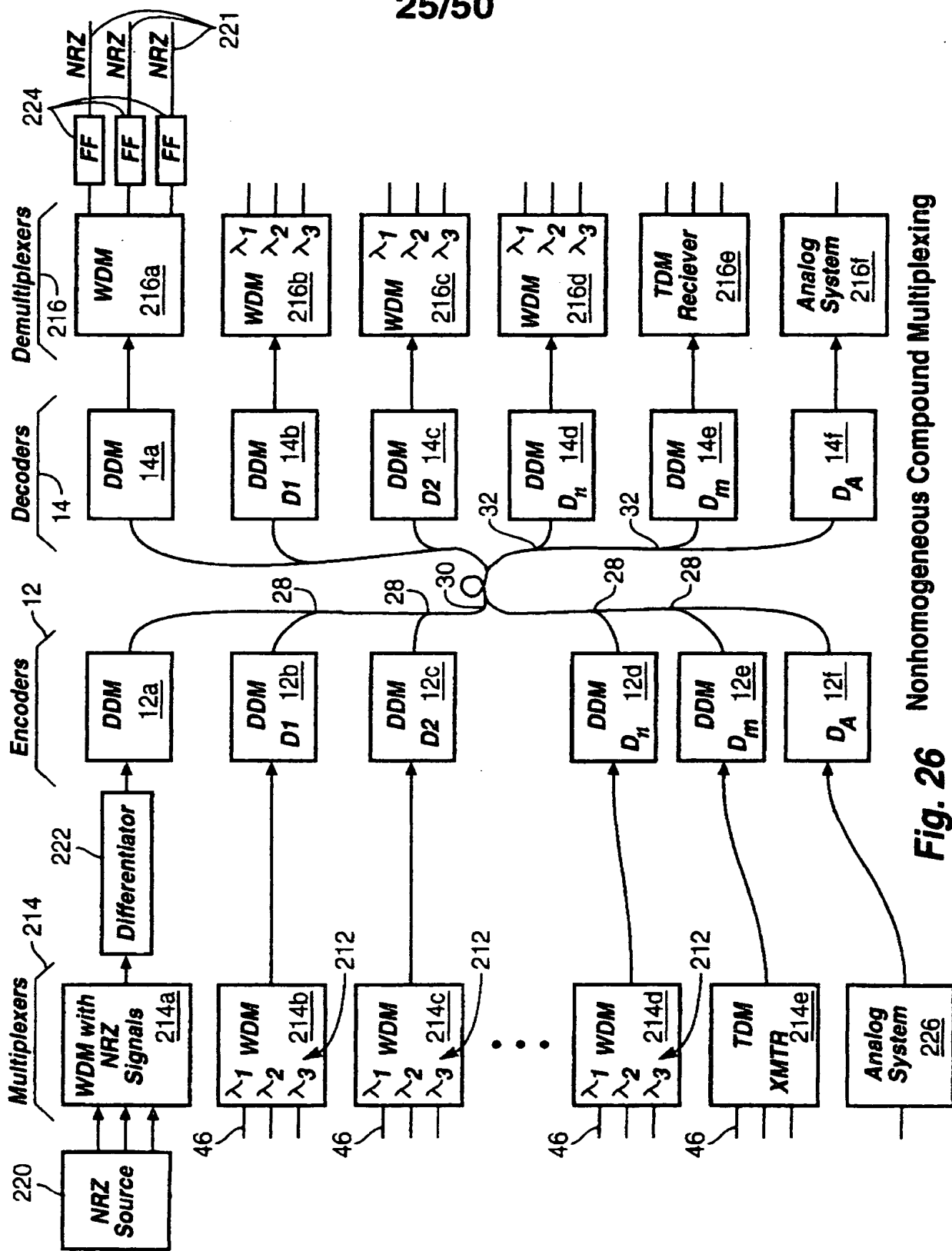
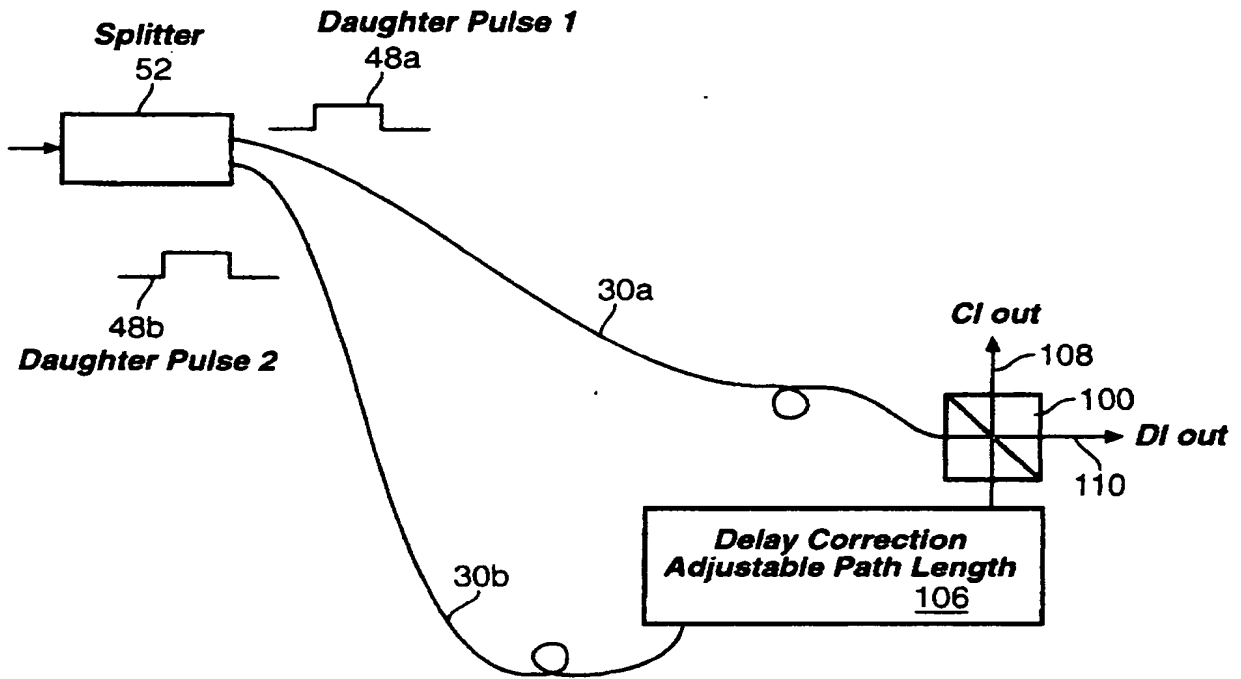


Fig. 26 Nonhomogeneous Compound Multiplexing



**Multiple Delay Path
Integrated Delay and
Delay Correction**

FIG. 27

004227 00523460

Photonic NRZ Interface

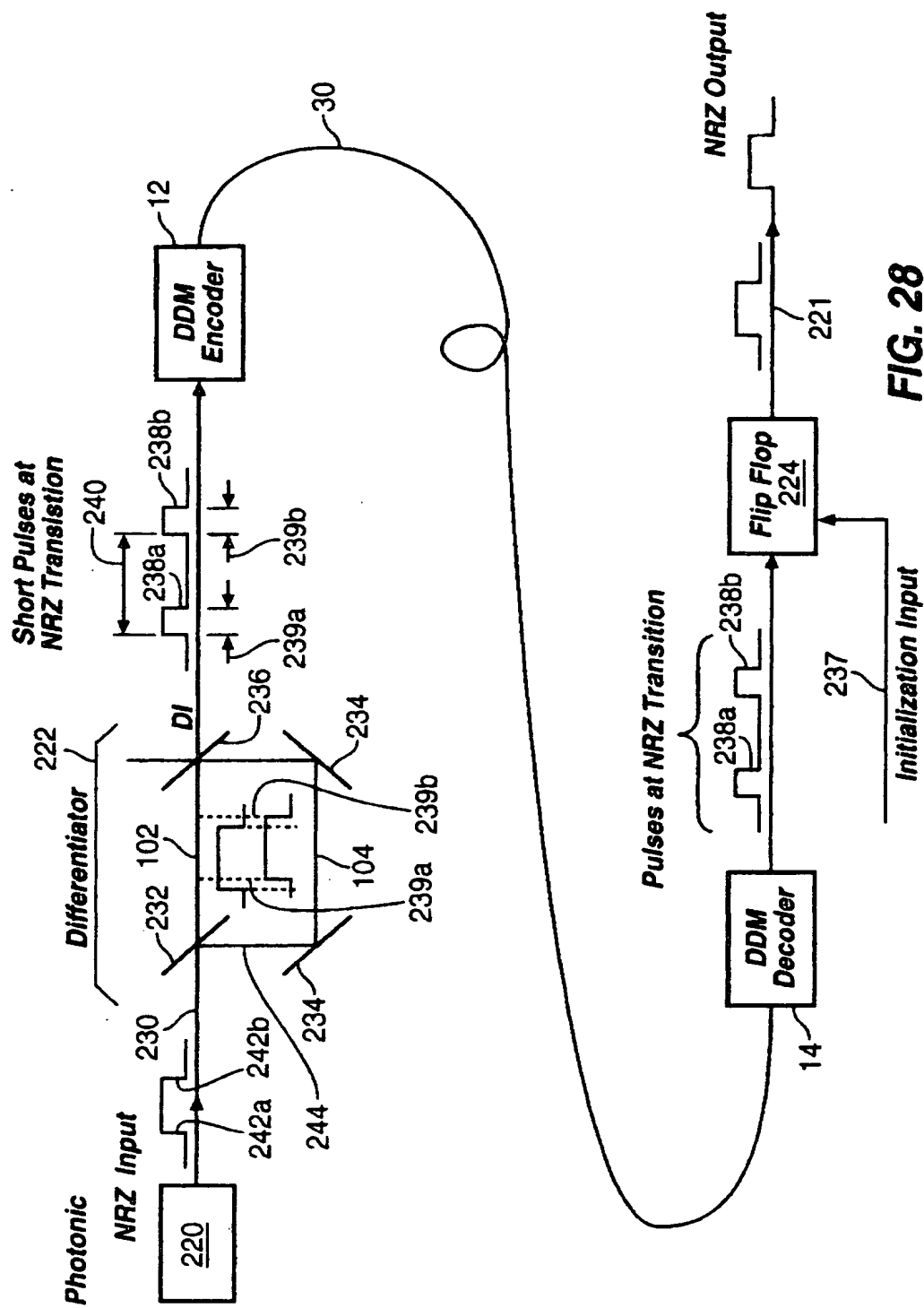


FIG. 28

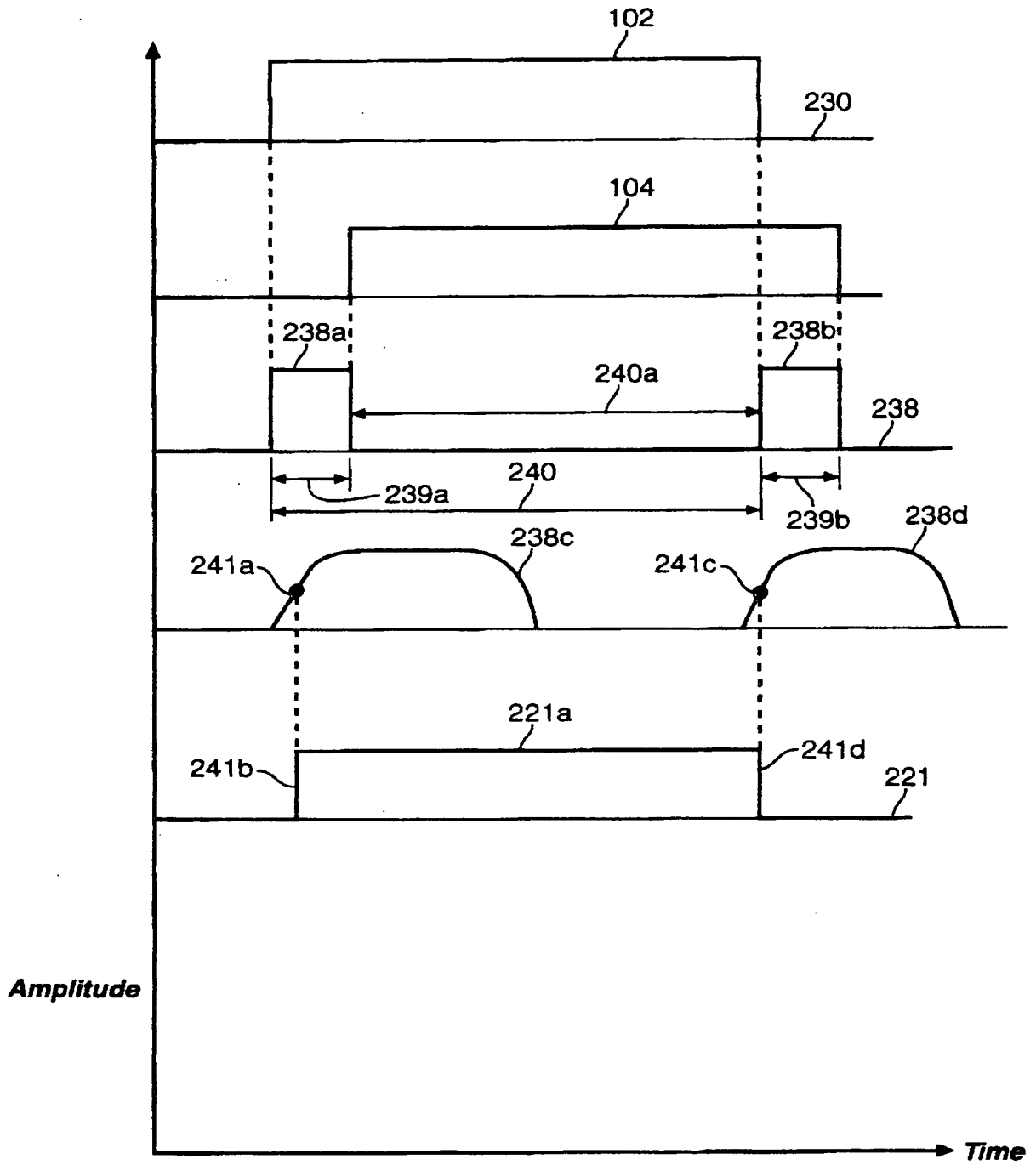
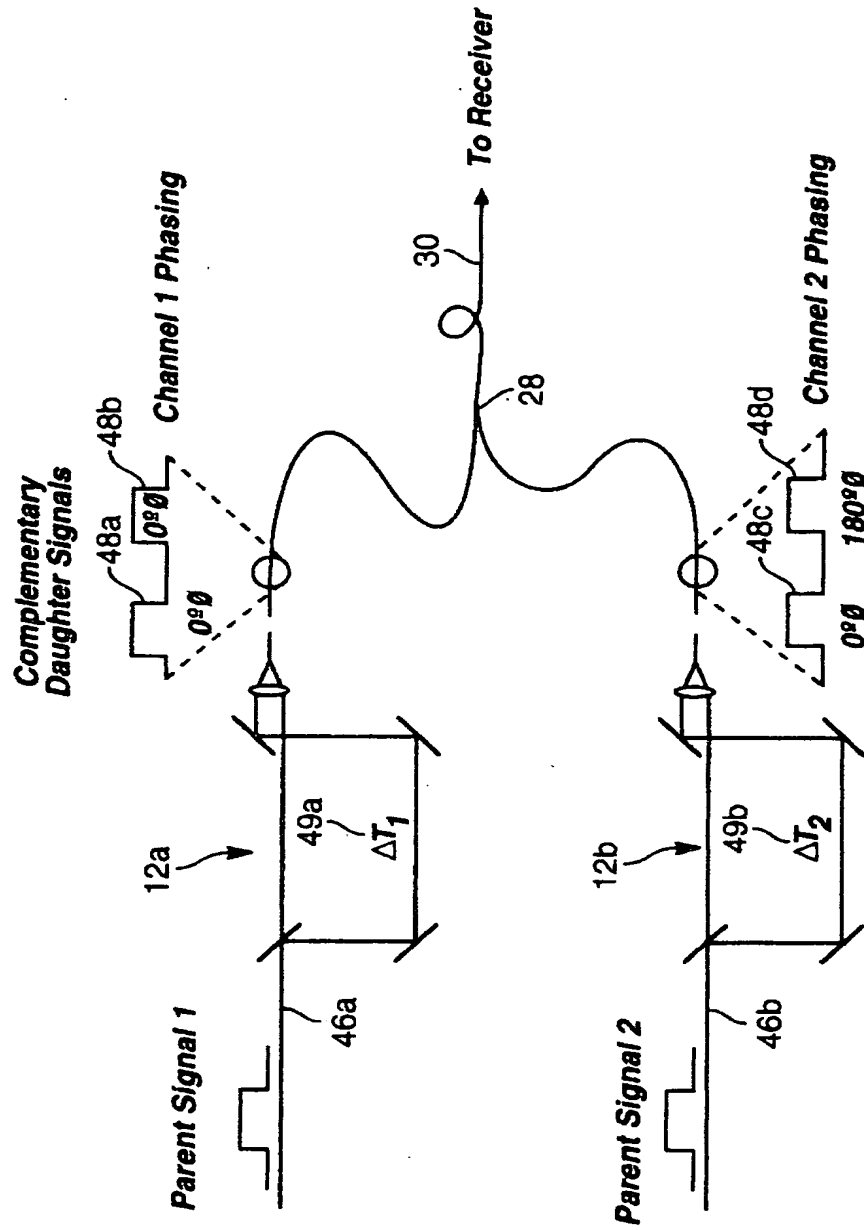


FIG. 29



Phase Sequenced Dual Channel Encoder

FIG. 30

Phase Sequence Timing

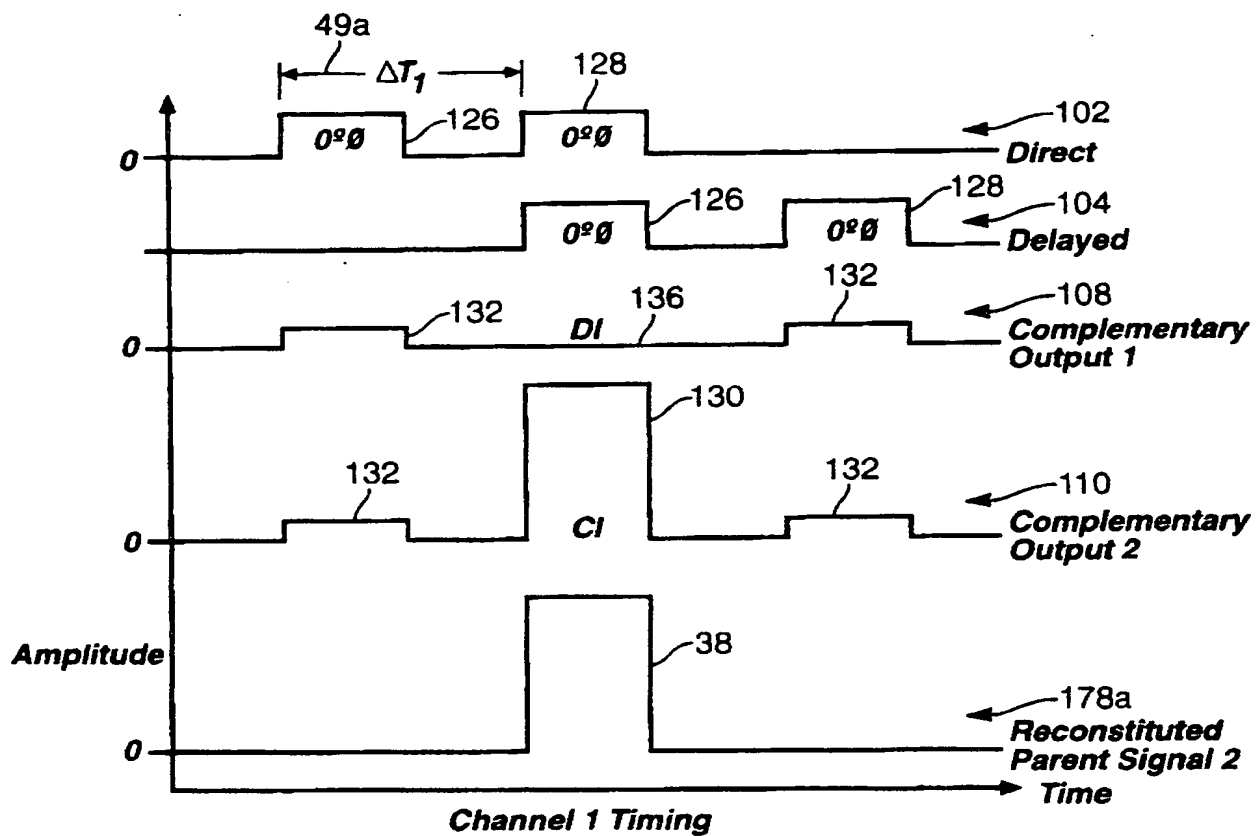


FIG. 32

Phase Sequence Timing

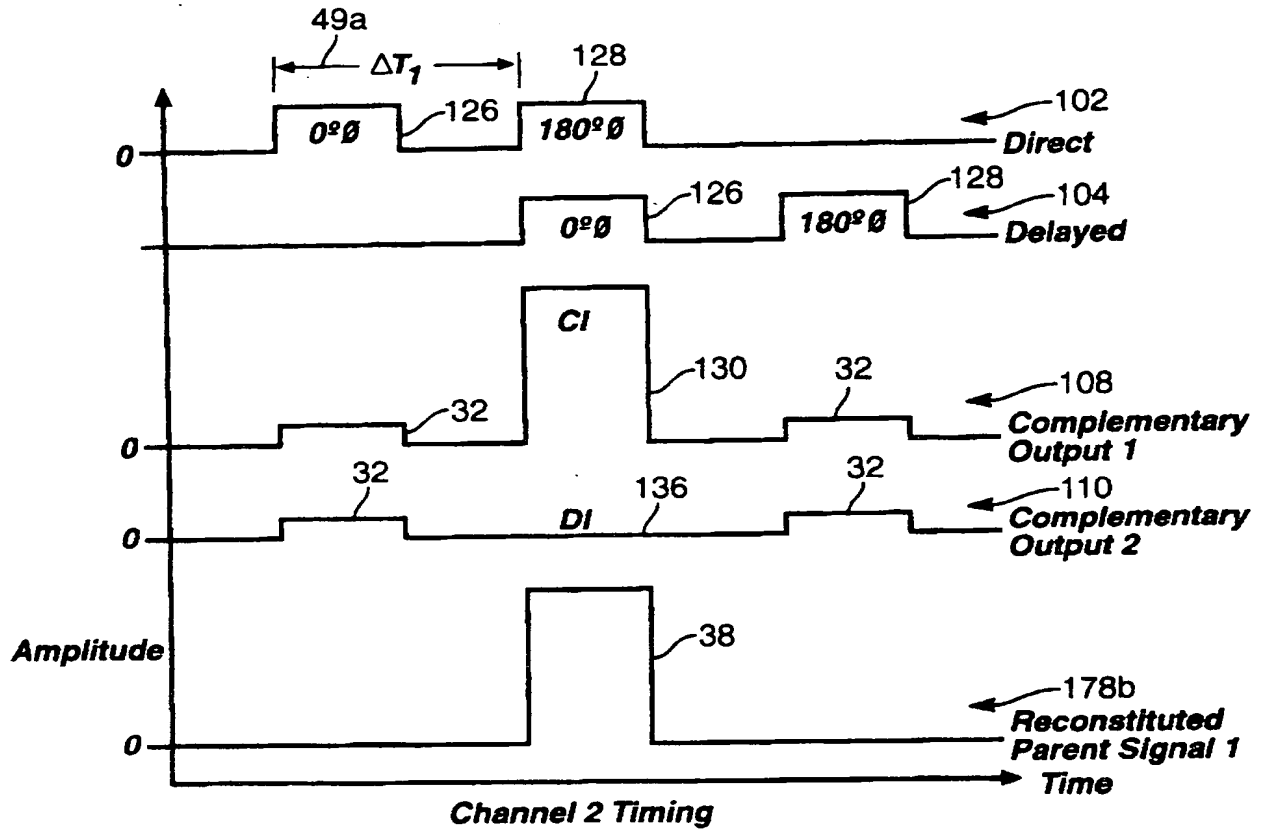


FIG. 33

Quadrature Encoding/Decoding Apparatus

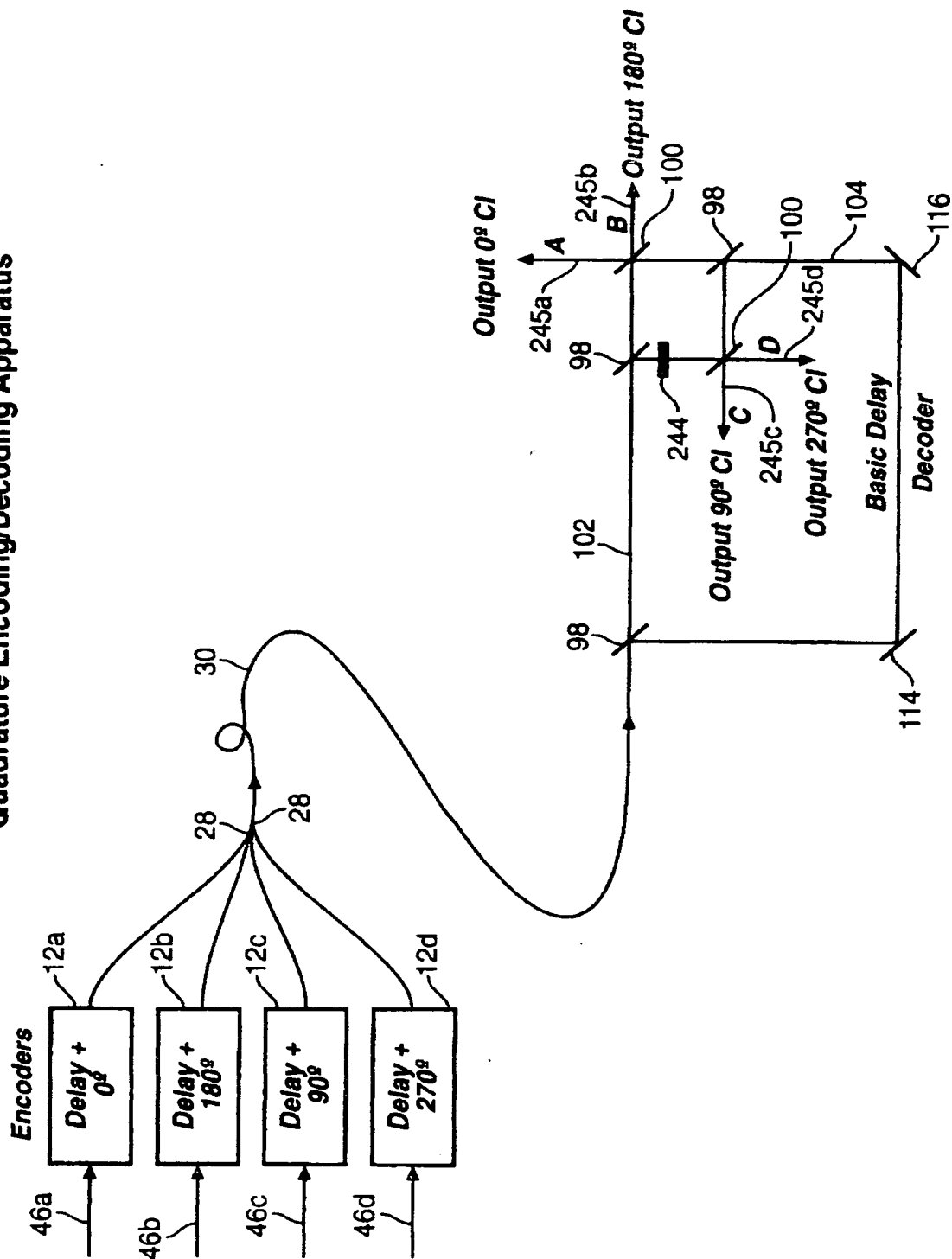


FIG. 34

46a
46b
46c
46d

Channel 1
Channel 2
Channel 3
Channel 4

Phase of Direct Signal	Phase of Delayed Signal	Quadrature Outputs			
		A	B	C	D
0	0	CI	DI	C = D	
0	180	DI	CI	C = D	
0	90	A = B		CI	DI
0	270	A = B		DI	CI

245a 245b 245c 245d

FIG. 35

Quadrature Wave Forms For One Channel

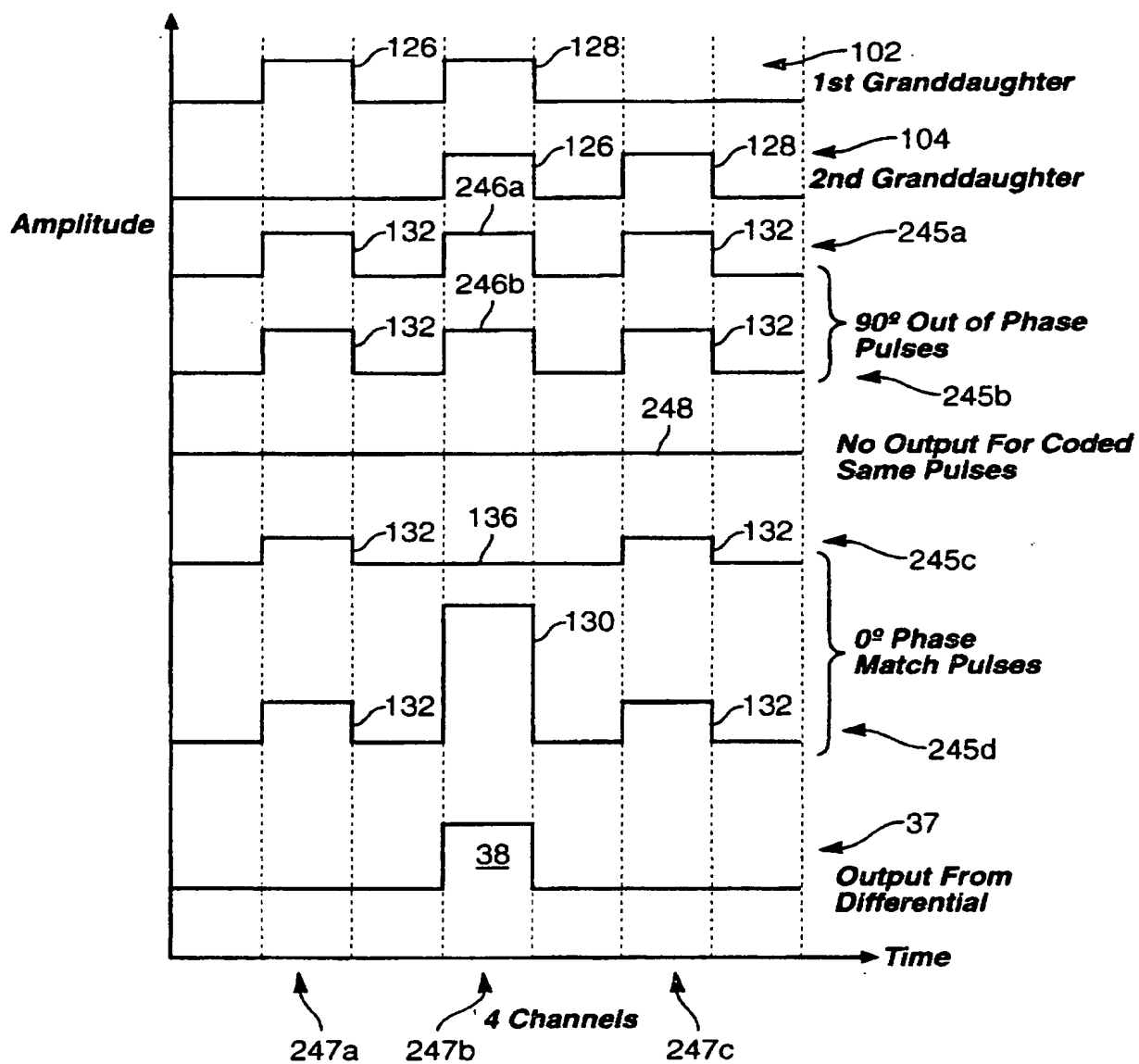


FIG. 36

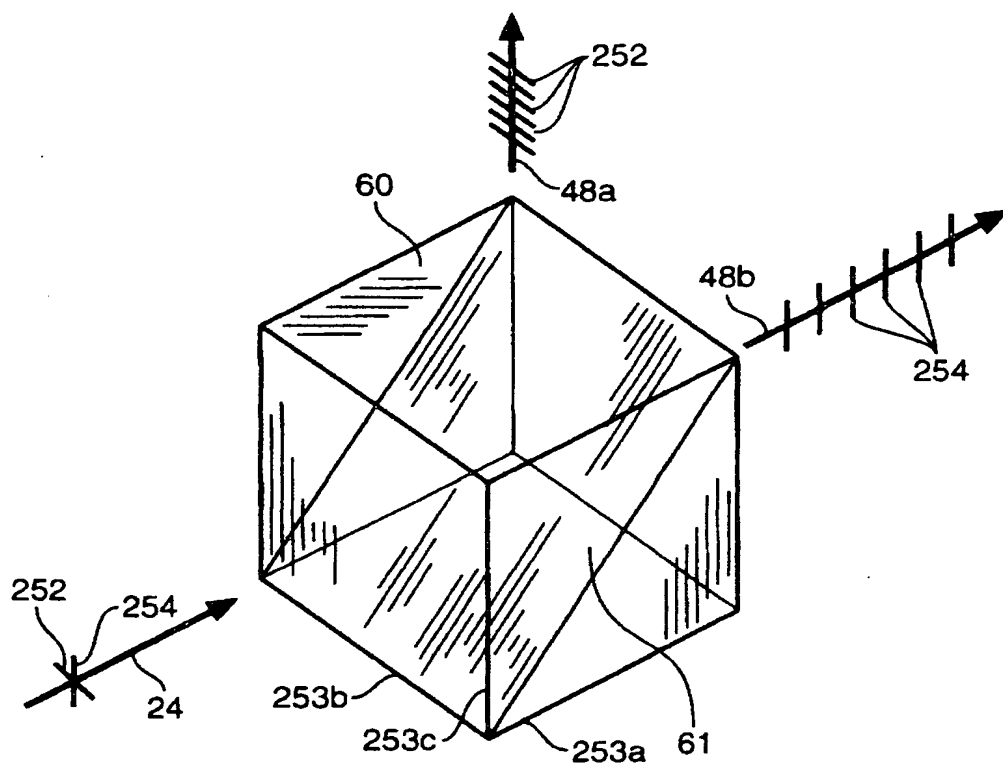
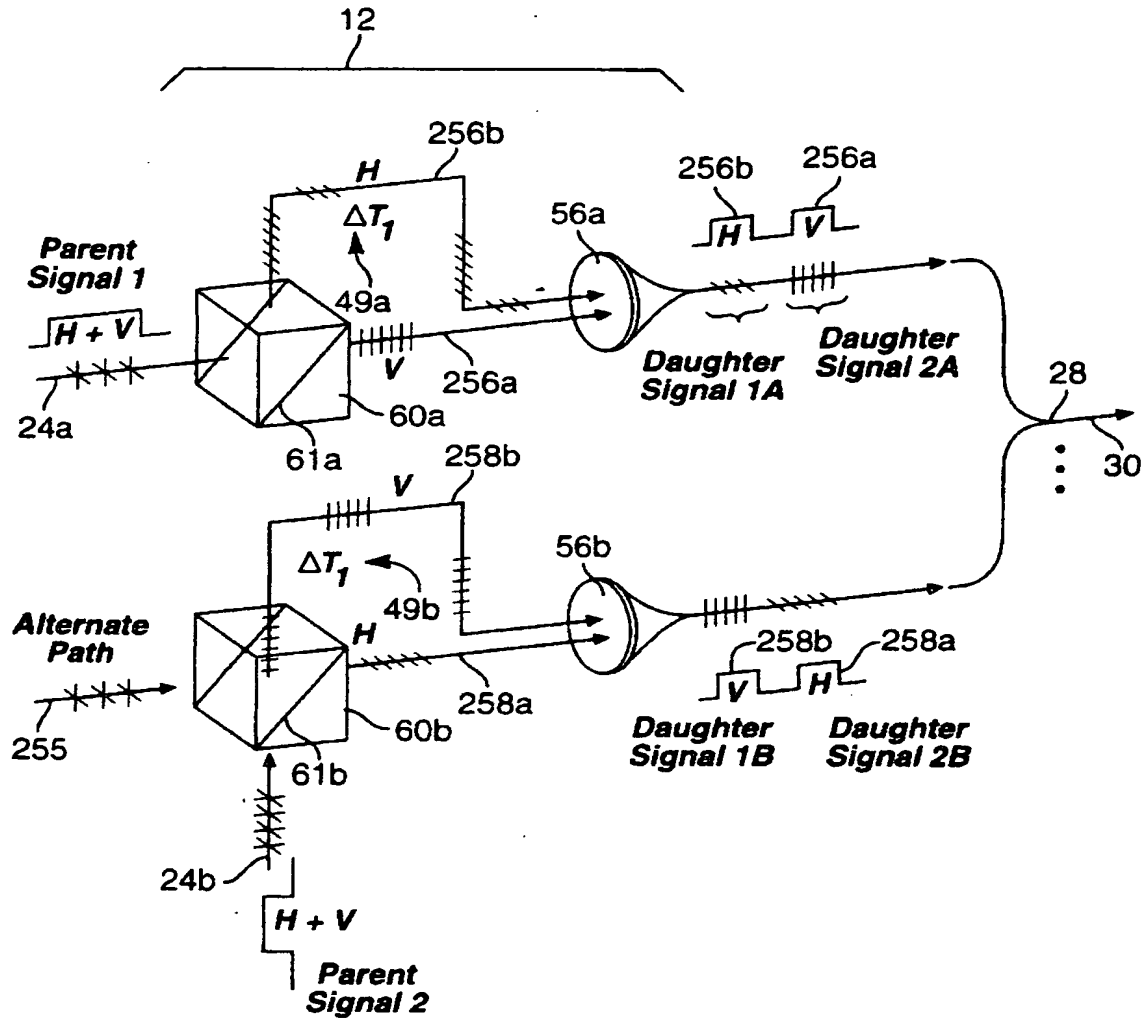


FIG. 37A



Double Encoder With Polarizations Sequenced to Differentiate 2 Channels Having the Same Time Delay Between Daughter Signals

FIG. 38



FIG. 39



FIG. 40

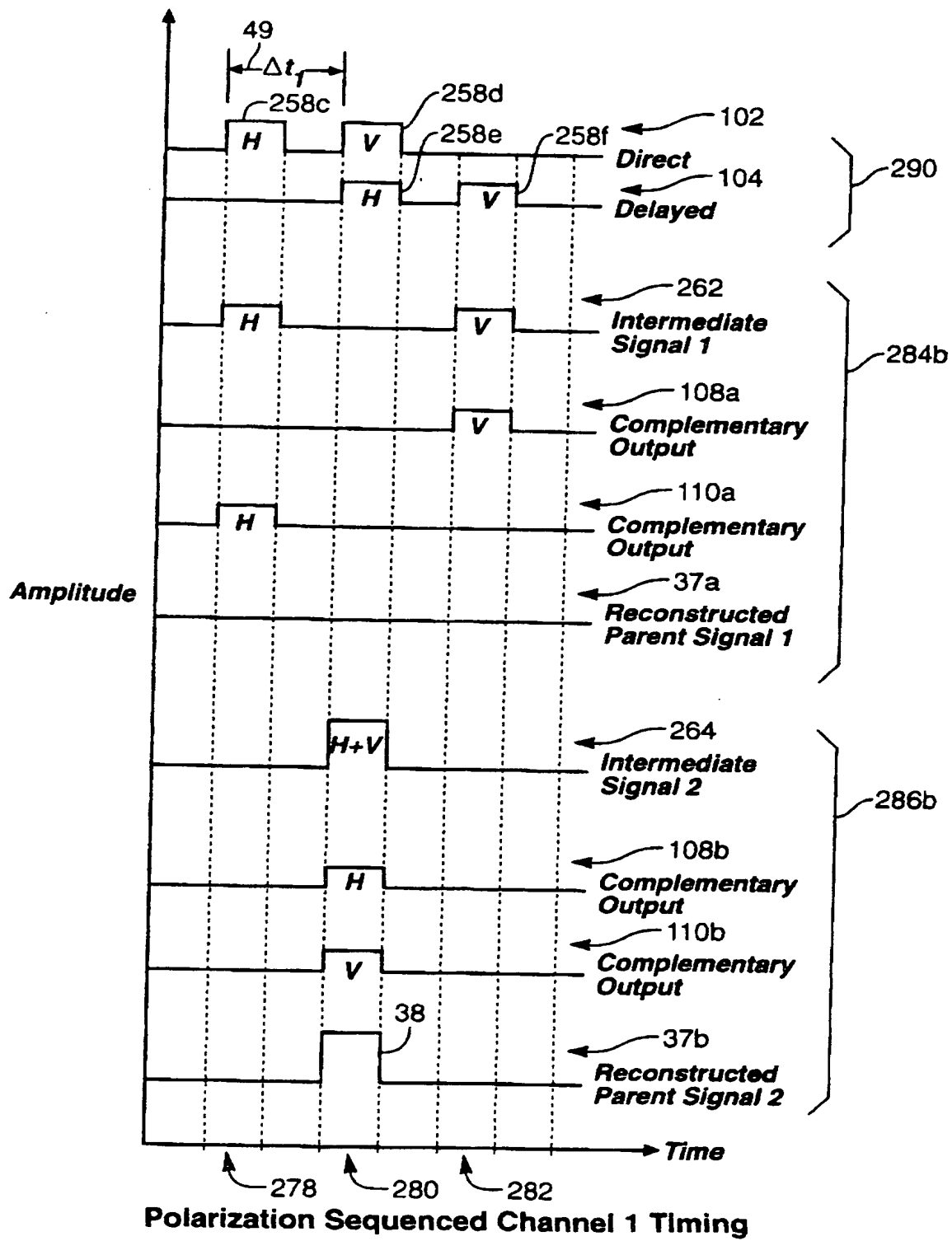
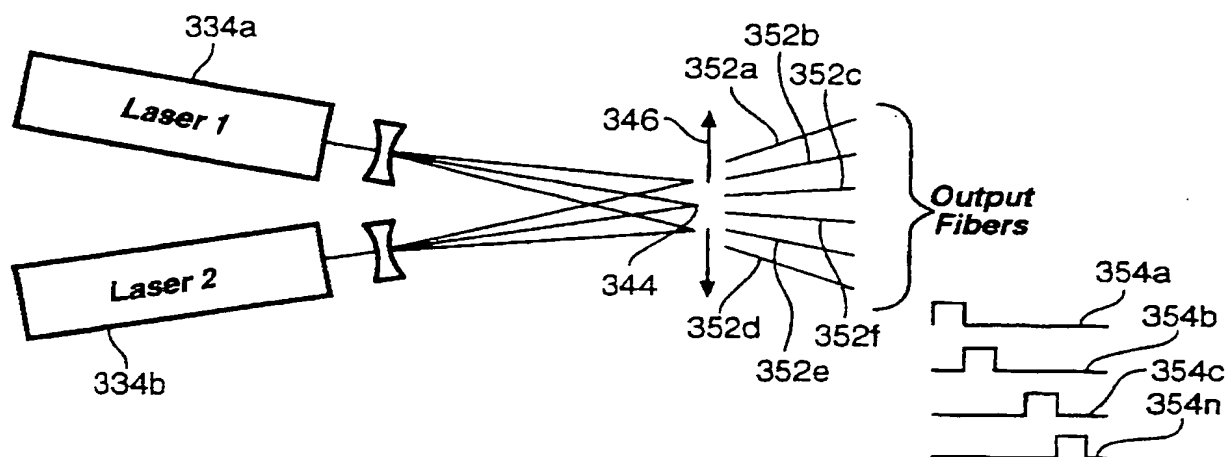






FIG. 43



**FIG. 46**

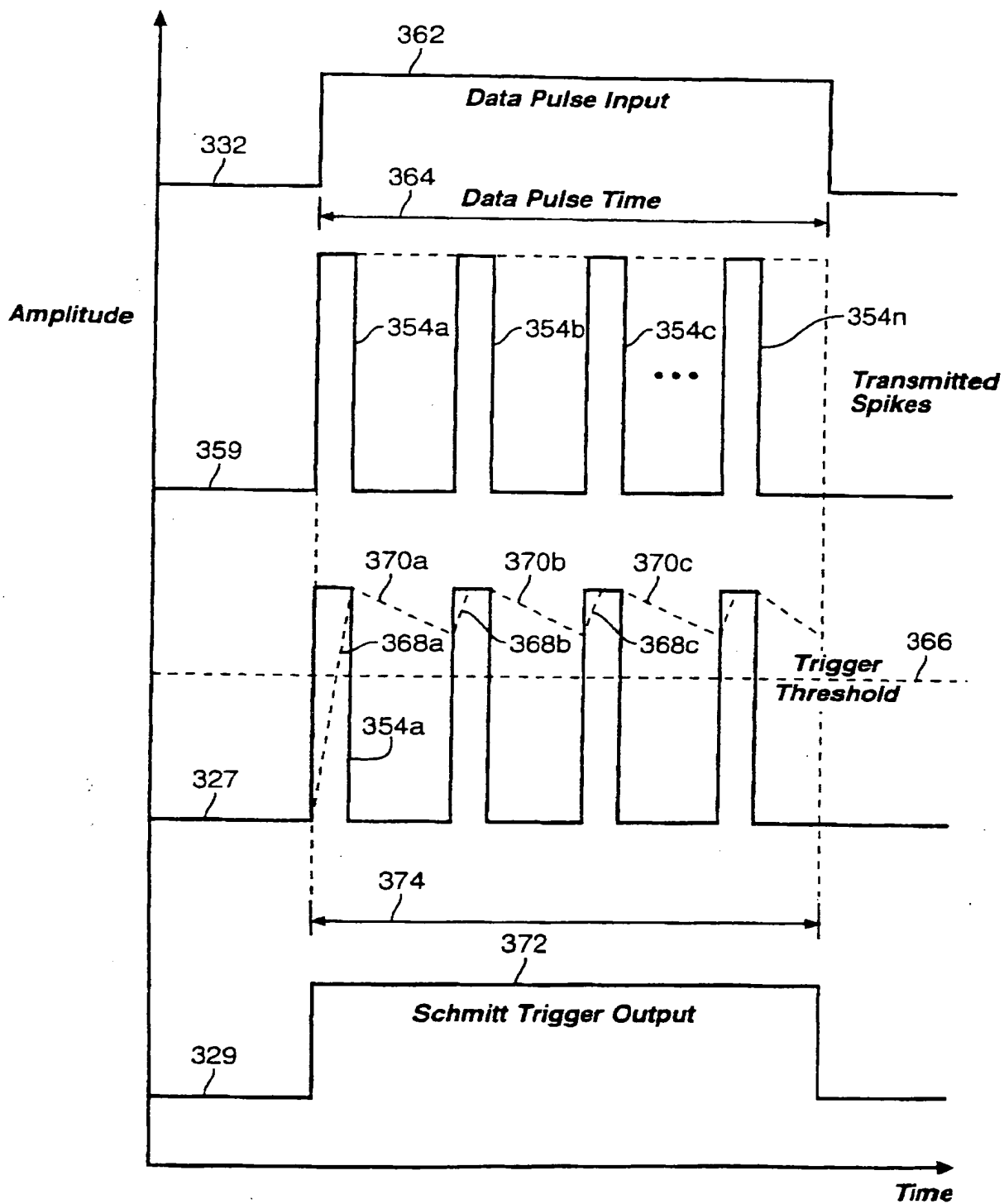


FIG. 47

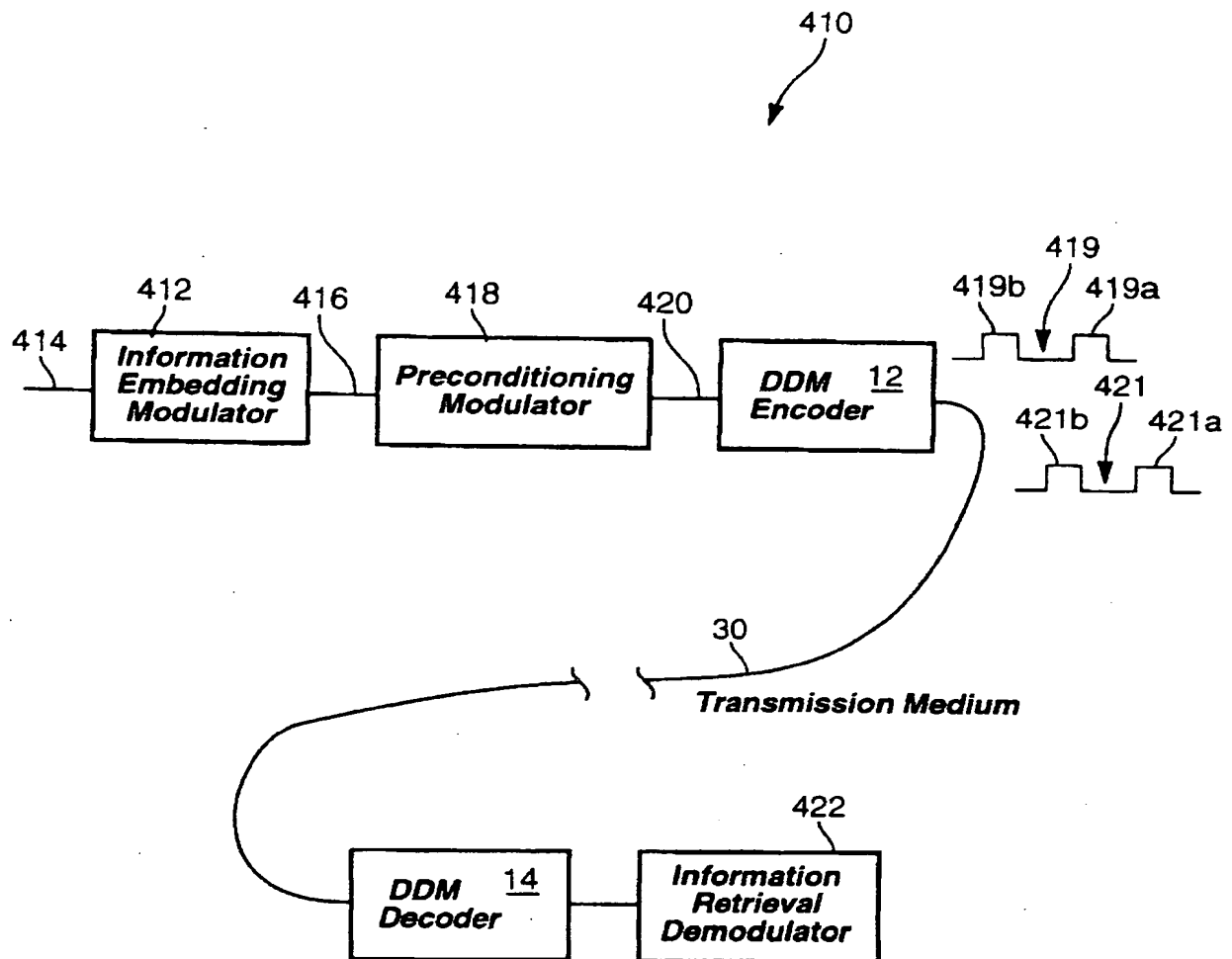
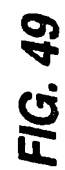


FIG. 48



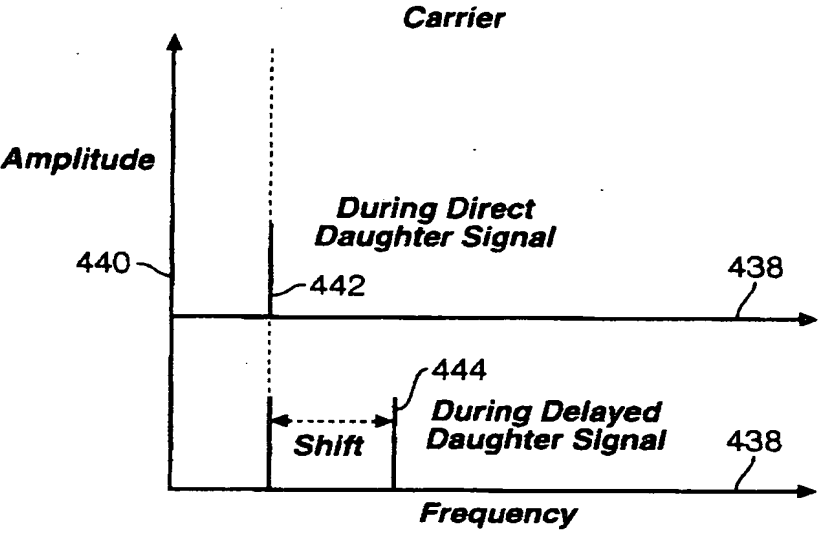


FIG. 50